

LeCroy

**ENET
Software Option**

Operator's Manual

March 2006



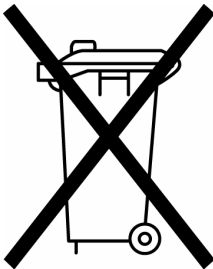
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INTRODUCTION

LeCroy's Ethernet test package (ENET) performs electrical tests for the three common networking standards over unshielded twisted pair (UTP) cables normally referred to as CAT5 or CAT5E. ENET performs electrical tests on 10Base-T, 100Base-TX, and 1000Base-T signals as specified in IEEE802.3-2000 and ANSI X3.263-1995 standards.

Compatibility

ENET is a software option that is compatible with the following LeCroy X-Stream™ oscilloscopes:

- All WaveMaster series oscilloscopes
- All SDA series Serial Data Analyzers
- WavePro 7100, 7200, 7300
- WaveRunner 6200

Oscilloscope bandwidths less than 1 GHz, therefore, are not recommended for these standards.

Ethernet Test Fixtures

Test fixtures are required to connect the signal under test to the oscilloscope running the ENET software. The fixtures are available from LeCroy (part number TF-ENET and TF-10BT) and provide a means to probe the device under test via a standard RJ45 plug or jack. TF-ENET includes two fixtures (pass-through and terminated) along with removable terminations. These fixtures are shown below (Figure 1). The second set of test fixtures (TF-10BT) provides the "twisted pair model" described in IEEE802.3-2000 clause 14.3.1.2 for testing 10Base-T signals along with three loads (Figure 2).

The use of these fixtures for measuring each standard is described in the respective sections of this manual.

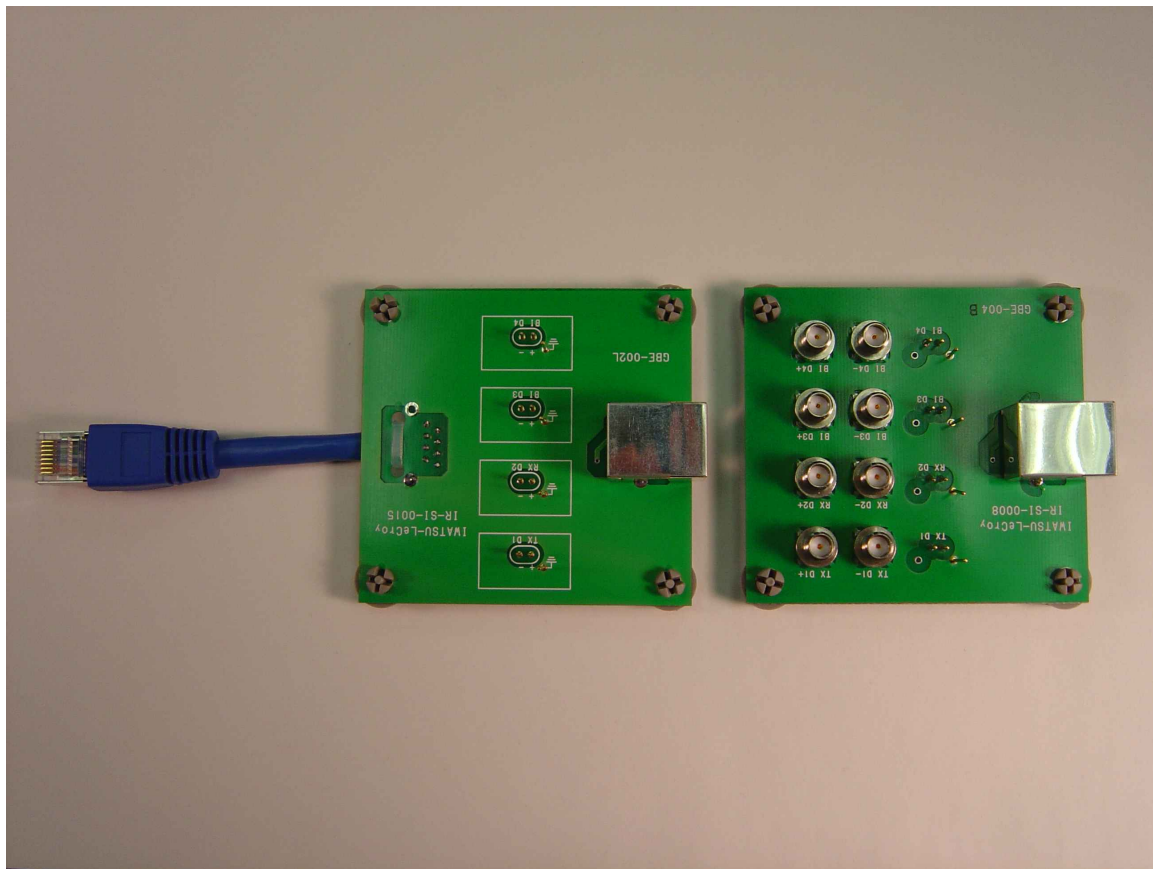


Figure 1: Ethernet fixtures for testing 100Base-TX and 100Base-T (TF-ENET). The fixture on the left (GBE-002L) allows jitter measurements to be made on an active link while the fixture on the right (GBE-004B) is used for terminated measurements for 100Base-TX and 1000Base-T.

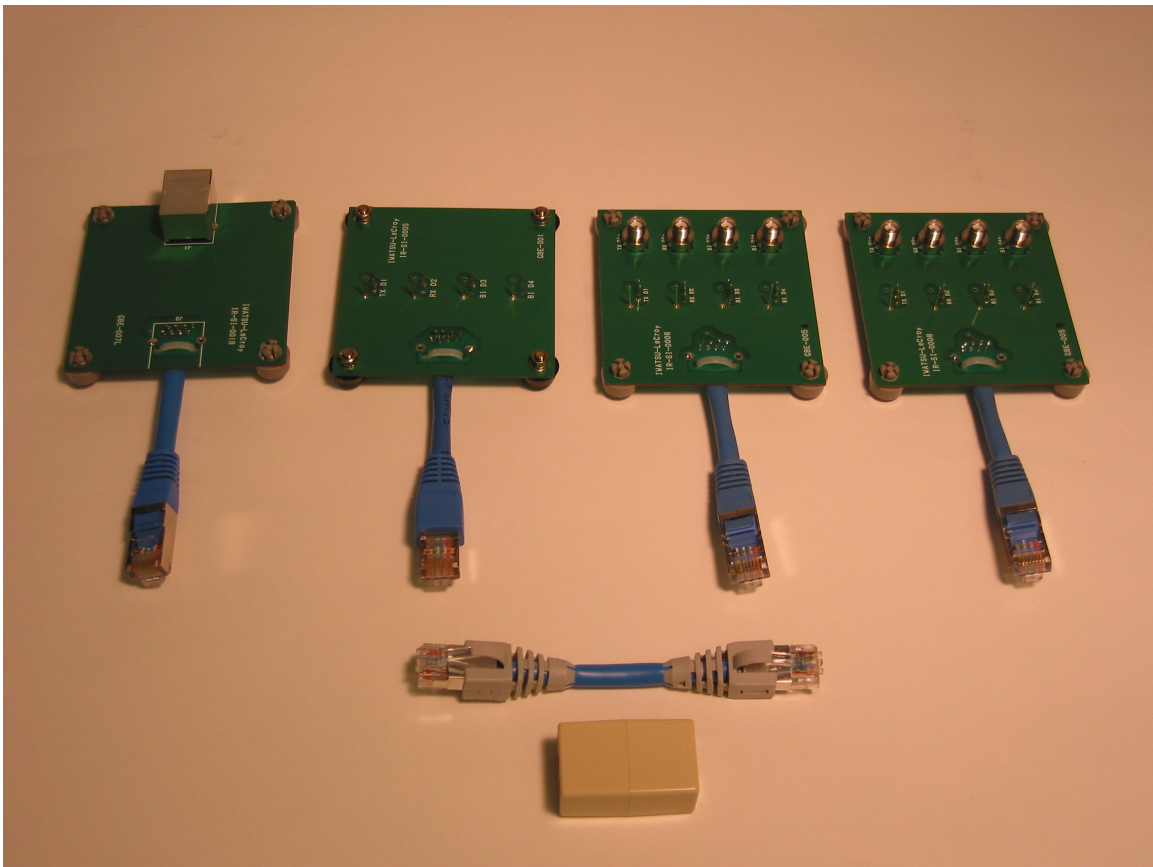


Figure 2: Fixtures for probing 10Base-T (TF-10BT). The twisted pair model (GBE-007L) is on the left, followed by test loads 1, 2 and 3 (GBE-001, GBE-005B, GBE-005A). The female-to-female RJ45 connector is used to attach the twisted pair model to the test loads and the short section of RJ45 cable is used to connect the twisted pair model to the device under test.

Probing

The ENET software package and fixtures support two methods of probing the signal under test. Direct probing is accomplished by attaching the signals from the fixture directly to the oscilloscope channels, using coaxial cables. It is also possible to use an active differential probe of suitable bandwidth. A system bandwidth of at least 2 GHz is required for measuring 100Base-T and 1000Base-T signals.

The compliance tolerances for 100Base-T and 1000Base-T are very tight (1% for many measurements). In order to achieve the best results, it is recommended that direct probing be used whenever possible to minimize the noise and distortion of the measurement system. For this reason, direct probing is the method described in this manual.

Recommended LeCroy Probes

- D350-ST-SP
- D300A-AT
- HFP2500

Documenting Test Results

Documentation is always an important consideration when performing any compliance test. The LeCroy ENET package displays all parameters for each measurement on the instrument screen along with pass/fail indicators and the appropriate waveforms. Each step can be saved by pressing the print screen button after the completion of the measurement.

The print screen function is set up in the **File, Print Setup...** menu as shown below. The file format can be JPEG, PNG, bitmap, TIF, or Adobe™ Photoshop. The file name can be set to some descriptive name for example, “device 0001 test”. The file name cannot end in a number because the system will automatically append a number to the name which will be incremented each time the **Print Screen** button is pressed. The **Use Print Colors** control, when checked, prints the grid area on a white background rather than a black one. The hardcopy area should be set to “DSO Window” so that the measurement description is included in the image. The **Directory** control allows the user to select where the files are stored. This can be any directory either on the internal hard disk, a removable media (USB memory stick, etc.), or a network drive.

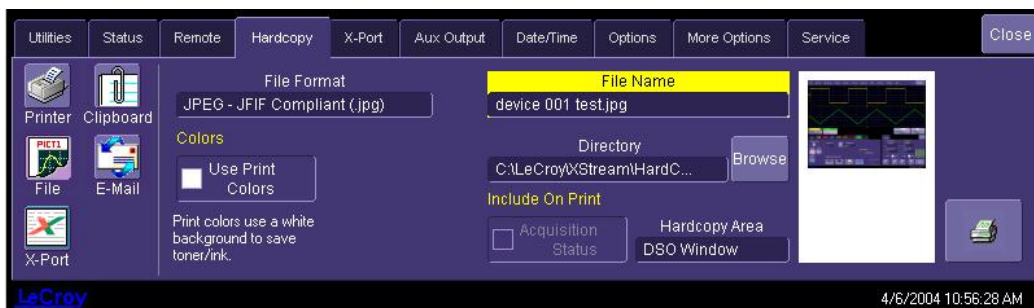


Figure 3: Print setup menu



Figure 4: Print Screen button on instrument front panel

INSTALLATION

You must purchase an option key to enable the ENET option. Call LeCroy Customer Support to place an order and receive the code.

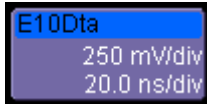
To enter the key and enable the purchased option, proceed as follows:

1. From the menu bar, select **Utilities**, then **Utilities Setup...** from the drop-down menu.
2. Touch the **Options** tab, then the **Add Key** button.
3. Use the pop-up keyboard to enter the key code.

The oscilloscope must be restarted in order to activate the option after installation. Once activated, Ethernet testing can be accessed by selecting **Analysis** from the menu bar, then **Ethernet Tests...** from the drop-down menu.

OPERATION

The main menu pictured below will be displayed at the bottom of the oscilloscope screen. The four buttons on the left (10Base-T, 100Base-TX, 1000Base-T, and OFF) allow you to select the standard to be tested. If the Ethernet Tests dialog is closed at any time, you can redisplay it in its most recent state by selecting **Ethernet Tests...** from the **Analysis** menu or by touching the ENET waveform descriptor label at the bottom-left of the screen, if it is displayed:



The name in the title bar of the descriptor label indicates the measurement waveform. For the case above, the descriptor label is "E10Dta".



Figure 5: ENET Main Menu

Source selection fields are displayed on the right side of the menu. The **Differential Data on 2 Channels** checkbox sets the oscilloscope to use two channels to probe the differential pair. Two

controls for master TX_TCLK and slave TX_TCLK are used for the 1000Base-T mode 2 and mode 3 jitter tests, or are grayed out otherwise. When a differential probe is used, the channel to which the probe is connected is selected in the “Source for + Data” field.

The following sections describe the use of ENET software option for testing 10Base-T, 100Base-TX, and 1000Base-T signal types.

10Base-T Tests

The required tests for the 10Base-T signal type consist of pulse mask, voltage level, and jitter. The requirements are given in the IEEE802.3-2000 standard in clause 42. The mask test requires the use of a “twisted pair model,” which in effect is a low-pass filter that models the effect of transmitting the signal over a standard CAT5 cable. This twisted pair model is available from LeCroy (part number TF-10BT pictured above).

1. Touch the **10Base-T** button on the left side of the menu to select the 10Base-T test mode.
2. Check the **Differential Data on 2 Channels** checkbox if you are probing with two separate channels and enter the desired channels into the appropriate fields.
3. Enter the channel to which the differential probe is connected in the “Source for + Data” field if you are not using this option.

The test fixtures allow for probing either with a differential probe or by connecting each wire in the pair to a separate channel. Use the fixture GBE-004B in the TF-ENET fixture set (Figure 1) to probe the signal using two channels. The test loads in the TF-10BT fixture set, however, require the use of a differential probe.

The 10Base-T transmitter is tested at the output of the media access unit (MAU). This connection is made using an RJ45 twisted pair connection. The MAU can be internal or external to the transmitter; and there are different requirements for each type of MAU. The ENET software provides separate masks for each type of MAU to accommodate these different requirements.

10Base-T DOV Mask and Voltage Test

The differential output voltage (DOV) is defined as the absolute value of the peak differential voltage measured into a 100 ohm termination. The mask test evaluates the pulse shape.

1. Set up the device under test by attaching the output of the MAU to the input RJ45 jack of the twisted pair model (GBE-007L) using a short section of RJ45 cable. The output of the twisted pair model is connected to the terminated fixture (GBE-001).
2. Connect a differential probe to the pins marked **TX D1**.

The transmitter should be set to generate a pseudo random bit pattern of at least 511 bits in duration. This type of pattern will repeat every 511 bits or more so that over a shorter measurement time, the data will appear to be random.

Note: The method for setting the device under test into transmit mode is device specific. Contact your PHY chip vendor for information on how to do this.

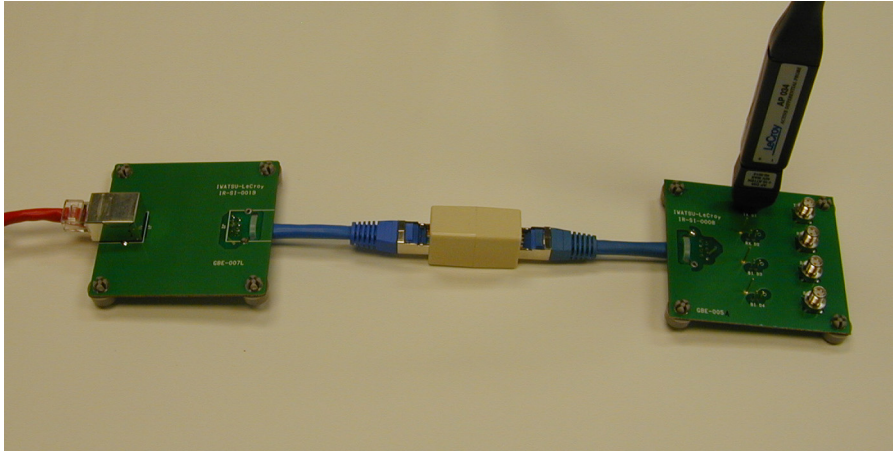


Figure 6: Fixture connections for 10Base-T mask test using the twisted pair model (GBE-007L). The load pictured on the far right is the GBE-005B (load 1). This test must be performed with three different loads GBE-001 (terminated), GBE-005A (load 2) and GBE-005B (load 1). The connection to the device under test is made using the RJ45 connector at the left of this picture.

1. From the menu bar, select **Analysis**, then **Ethernet Tests...** from the drop-down menu. Touch the 10Base-T button at the left side of the **Ethernet tests** menu.
2. Select the appropriate mask from the “Select Test” field:
 - DOV Mask MAU Ext for external MAU testing
 - DOV Mask MAU Ext Inv for external MAU testing of the negative-going pulses
 - DOV Mask MAU for internal MAU testing
 - DOV Mask MAU Inv for internal MAU testing of the negative-going pulses

Only two of the four masks above will be used for any given device (either internal or external MAU). Both positive and negative-going pulses must be tested.

3. Select the channel to which the differential probe is attached in the “Source for + Data” field.
4. Click the **Set Up and Start Test** button to start the test and display the pass/fail results.
5. Repeat the mask test for each of the test loads (GBE-001, GBE-005A, and GBE-005B) and for each pulse polarity (normal or inverted). There will be a total of 6 mask tests. Be sure to touch the **Set Up and Start Test** button after each test is selected.
6. Remove the twisted pair model from the MAU and connect the resistive load (GBE-001) directly to the MAU.
7. Attach the differential probe to the pins marked **TX D1** on the fixture.
8. Select **DOV Peak** in the “Select Test” field, then touch the **Set Up and Start Test** button.

The screen will change and the peak differential output voltage (DOV) will be measured. Parameter P1 indicates the peak voltage, and Q1 and Q2 test the upper and lower limits of this value.

9. Select "DOV Harmonics" in the "Select Test" field, then touch the **Set Up and Start Test** button. The display will show the Ethernet signal trace, and P1 will display the peak harmonic level in the power spectrum of the signal. The device under test should be transmitting an "all ones" pattern, which will be coded as alternating positive and negative going pulses. This waveform will give the worst case power spectrum with the highest level harmonics.



Figure 7: 10Base-T DOV Mask Test

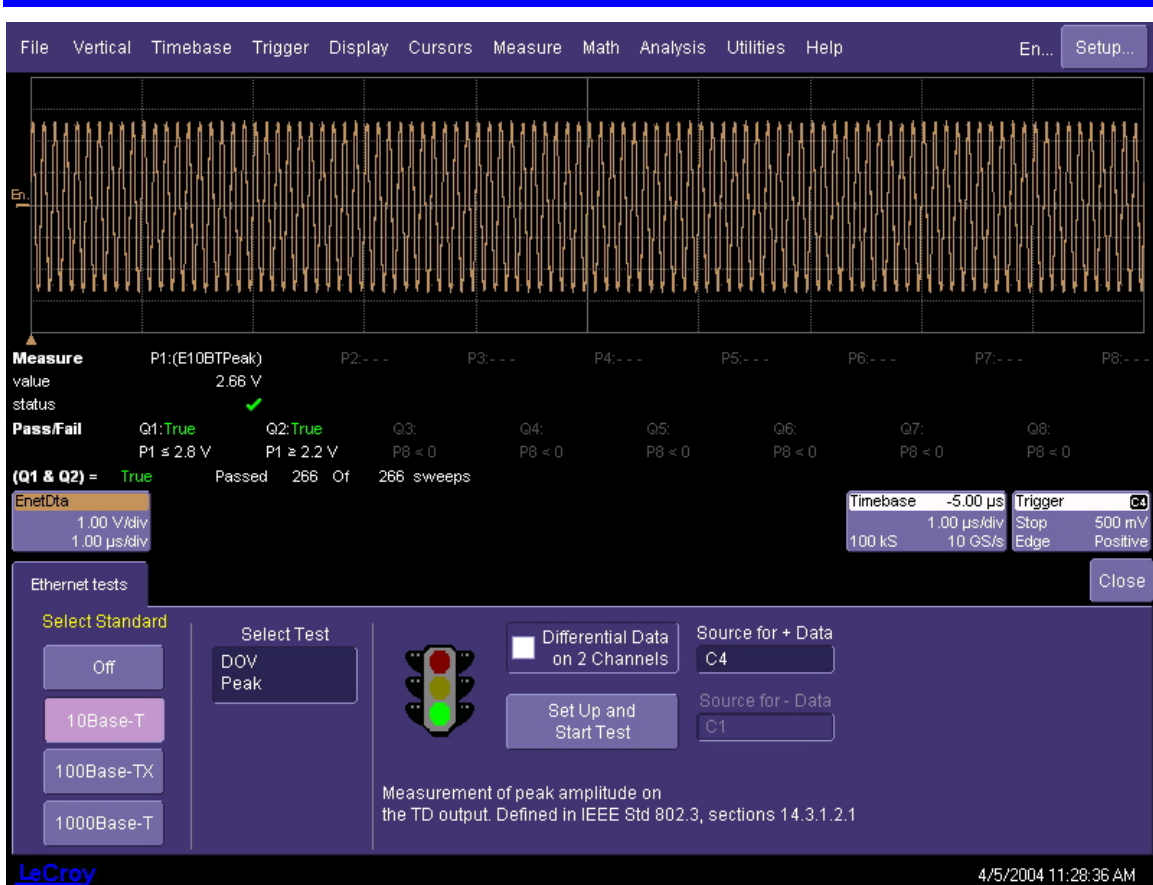


Figure 8: DOV Peak Voltage Test

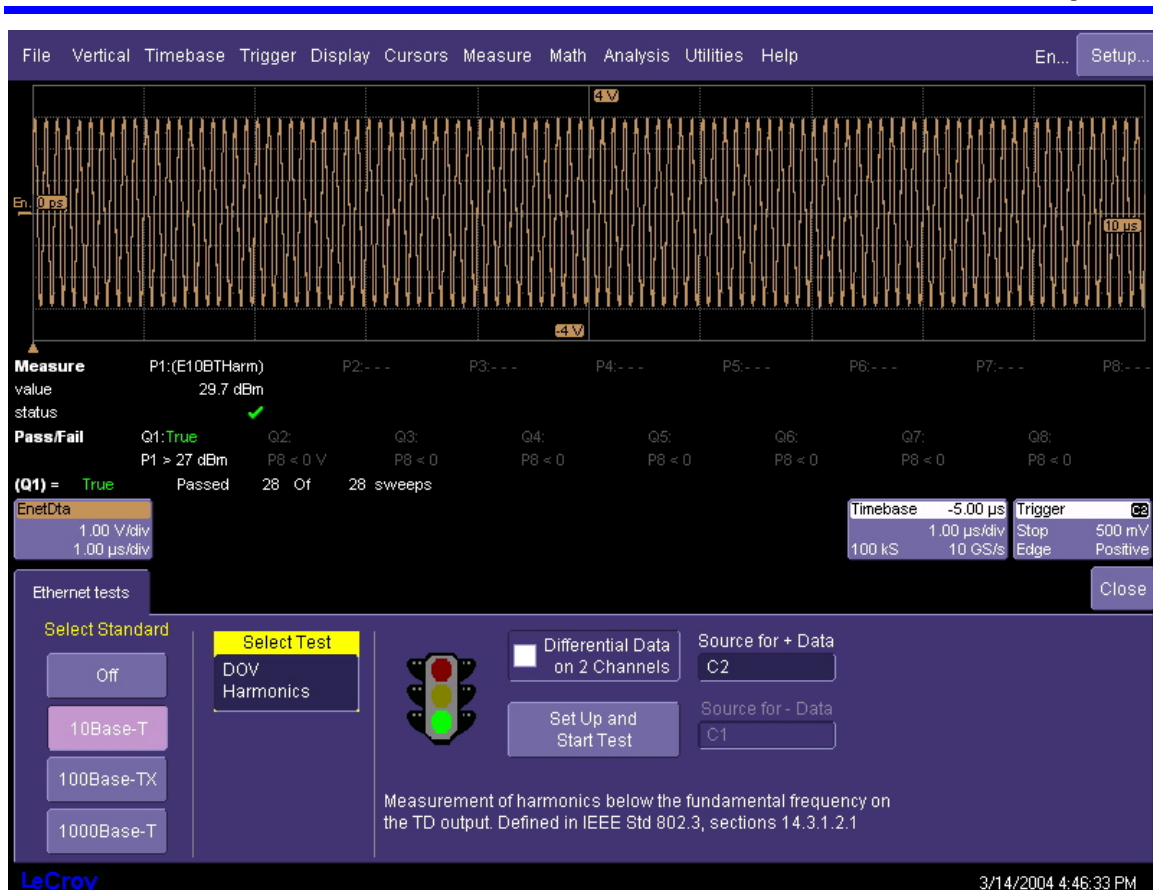


Figure 9: 10Base-T DOV Harmonics

10Base-T TP_IDL Mask Test

This test measures the wave shape of the TP_IDL signal at the output of the MAU. This signal is sent over the interface to indicate that the device under test is ready to receive data. In this sense, the TP_IDL signal is an end-of-packet indicator. The TP_IDL begins with a positive transition and must remain at a positive voltage level for between 2.5 and 4.5 bit times before going negative. Once the signal goes negative (below -50 mV) it may not exceed +50 mV. The signal may not exceed +/- 50 mV after 45 bit periods. These requirements are built into the masks in the measurement software.

The masks are broken into two parts; head and tail. The head mask includes the limits from the first transition out to 20 bit intervals. The tail mask contains the requirements beyond 20 bit intervals. The mask test must pass for two different test loads and is performed with and without the twisted pair model.

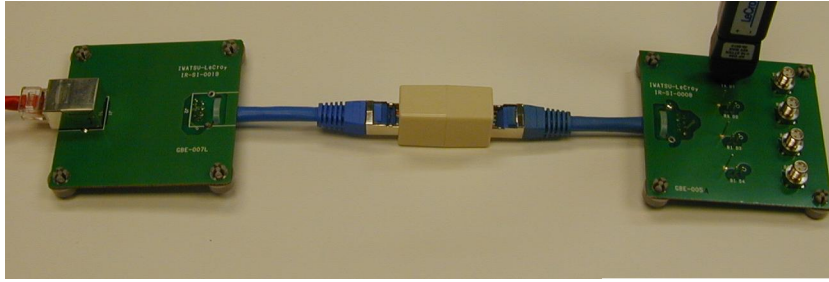


Figure 10: Fixture setup for TP_IDL test. The twisted pair model (GBE-007L) is shown on the left. The load shown is GBE-005A. Loads GBE-005B and GBE-001 must also be used. The device under test is connected to the RJ45 jack on the left of the picture.

1. Connect the twisted pair model fixture (GBE-007L) to the device under test.
2. Connect the output of the twisted pair model to test load 1 (GBE-005B).
3. Set the DUT to transmit pseudorandom data.

Note: The method for setting the device under test into transmit mode is device specific. Contact your PHY chip vendor for information on how to do this.

4. Touch the **10Base-T** button under “Select Standard.”
5. Enter the channel to which the differential probe is connected in the “Source for + Data” field.
6. Attach the differential probe to the pins marked **TX D1** on the test fixture.
7. Select **TP_IDL Head Mask** in the “Select Test” field.
8. Touch the **Set Up and Start Test** button to begin testing. The software will search for the TP_IDL pulse and center it within the mask automatically. You should check the **Average Result** checkbox so that the test is performed on an averaged waveform. Averaging reduces the noise in the trace.
9. Select **TP_IDL Tail Mask** in the “Select Test” field.
10. Touch the **Set Up and Start Test** button to begin testing.
11. Remove test load 1 from the output of the twisted pair model fixture.
12. Connect test load 2 (GBE-005B) to the output of the twisted pair model fixture.
13. Select **TP_IDL Head Mask** in the “Select Test” field.
14. Touch the **Set Up and Start Test** button to begin testing.
15. Select **TP_IDL Tail Mask** in the “Select Test” field.
16. Touch the **Set Up and Start Test** button to begin testing.

17. Remove the twisted pair model fixture and attach load 1 directly to the output of the DUT.
18. Select **TP_IDL Head Mask** in the “Select Test” field.
19. Touch the **Set Up and Start Test** button to begin testing.
20. Select **TP_IDL Tail Mask** in the “Select Test” field.
21. Touch the **Set Up and Start Test** button to begin testing.
22. Remove test load 1 from the output of the device under test.
23. Connect test load 2 (GBE-005B) to the output of the device under test.
24. Select **TP_IDL Head Mask** in the “Select Test” field.
25. Touch the **Set Up and Start Test** button to begin testing.
26. Select **TP_IDL Tail Mask** in the “Select Test” field.
27. Touch the **Set Up and Start Test** button to begin testing.

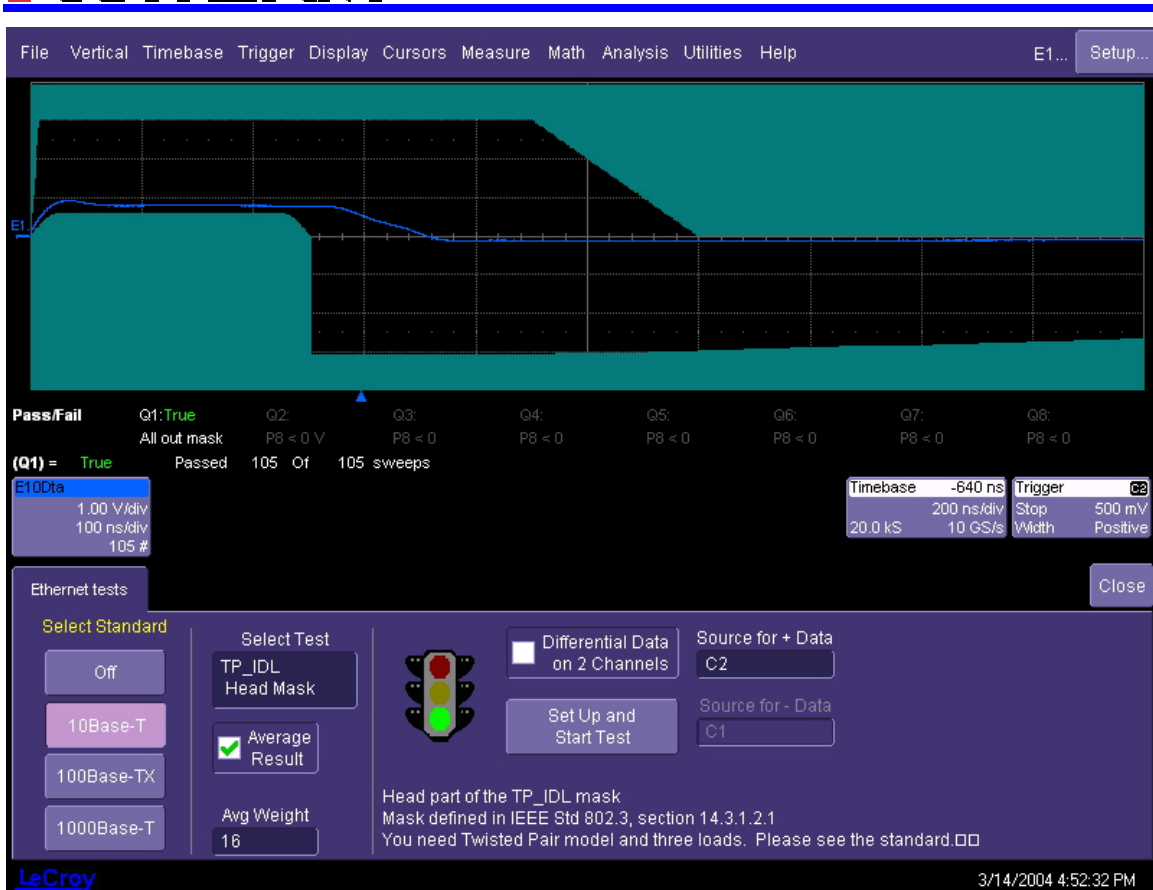


Figure 11: TP_IDL head mask test



Figure 12: TP_IDL tail mask test

Link Test Pulse Mask

The link test pulse is a single-bit positive-going pulse that is transmitted by the MAU whenever it is active, and before any traffic is present. This pulse is generated by a 10Base-T interface with no external connections. The link test pulse mask is similar to the TP_IDL mask except for its duration. The mask test is performed using the twisted pair model fixture (GBE-007L) and test loads 1 and 2 (GBE-005B and GBE-005A); and the test must pass for all conditions.

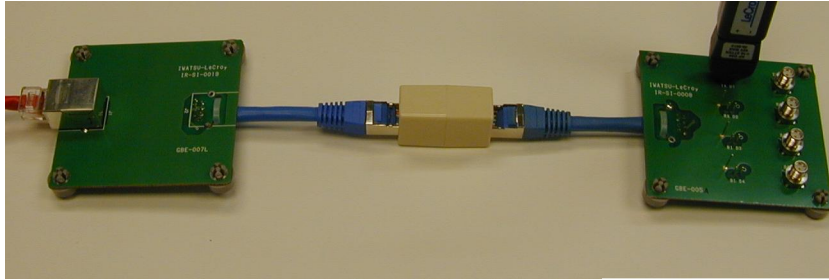


Figure 13: Fixture setup for link test pulse mask test. The twisted pair model (GBE-007) is shown on the left. The load shown is GBE-005A. Loads GBE-005B and GBE-001 must also be used. The device under test is connected to the RJ45 jack at the left side of the picture.

1. Connect the twisted pair model fixture to the device under test.
2. Connect the output of the twisted pair model to test load 1 (GBE-005B).
3. Attach the differential probe to the pins marked **TX D1** on the test fixture.
4. Apply power to the device under test. The link test pulse should appear on the oscilloscope screen.
5. Touch the **10Base-T** button in the “Select Standard” field.
6. Enter the channel to which the differential probe is connected in the “Source for + Data” field.
7. Select **Link Test Pulse Head Mask** in the “Select Test” field.
8. Touch the **Set Up and Start Test** button to begin testing. You should check the **Average Result** checkbox so that the test is performed on an averaged waveform. Averaging reduces the noise in the trace.
9. Select **Link Test Pulse Tail Mask** in the “Select Test” field.
10. Touch the **Set Up and Start Test** button to begin testing.
11. Remove test load 1 from the output of the twisted pair model fixture.
12. Connect test load 2 (GBE-005A) to the output of the twisted pair model fixture.
13. Select **Link Test Pulse Head Mask** in the “Select Test” field.
14. Touch the **Set Up and Start Test** button to begin testing.
15. Select **Link Test Pulse Tail Mask** in the “Select Test” field.
16. Touch the **Set Up and Start Test** button to begin testing.
17. Remove the twisted pair model fixture and attach load 1 (GBE-005B) directly to the output of the DUT.
18. Select **Link Test Pulse Head Mask** in the “Select Test” field.
19. Touch the **Set Up and Start Test** button to begin testing.

20. Select **Link Test Pulse Tail Mask** in the “Select Test” field.
21. Touch the **Set Up and Start Test** button to begin testing.
22. Replace load 1 with load 2 (GBE-005A).
23. Select **Link Test Pulse Head Mask** in the “Select Test” field.
24. Touch the **Set Up and Start Test** button to begin testing.
25. Select **Link Test Pulse Tail Mask** in the “Select Test” field.
26. Touch the **Set Up and Start Test** button to begin testing

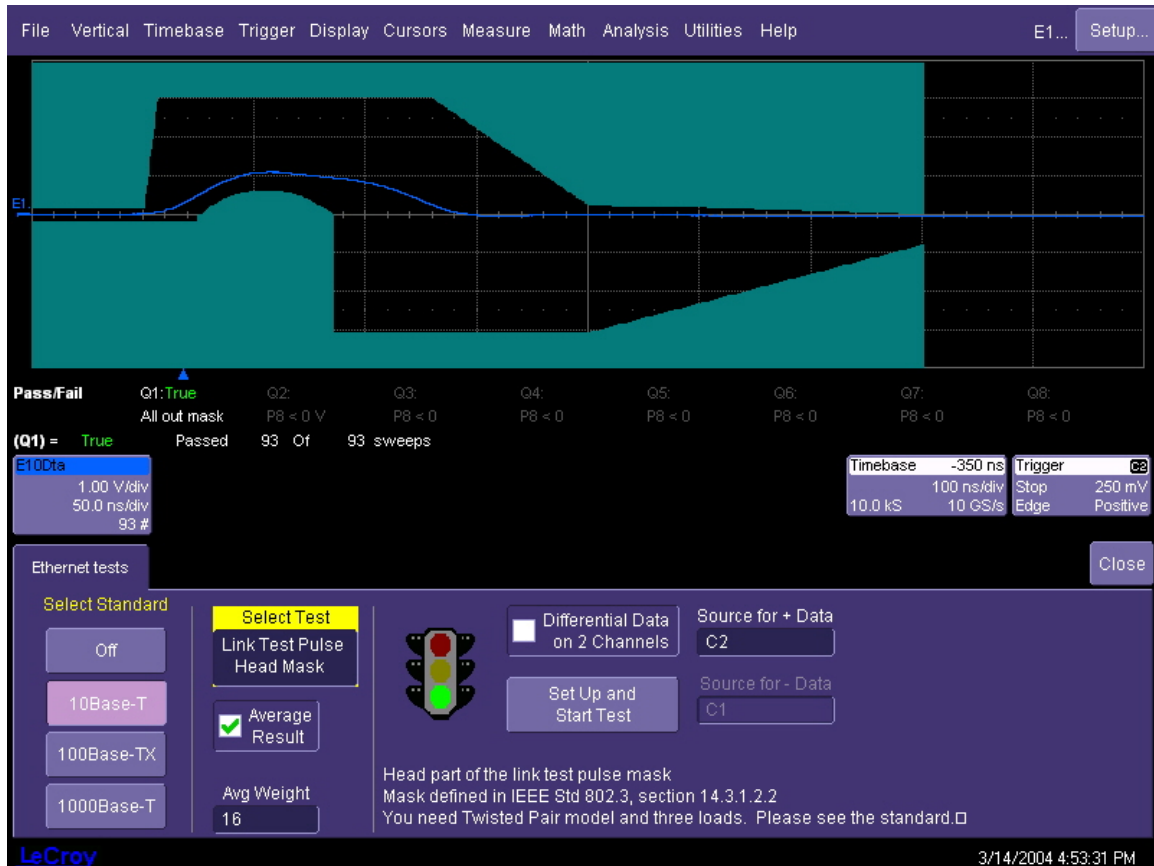


Figure 14: Link pulse mask test (head portion). This mask test must pass for three test loads, and with and without the twisted pair model (GBE-007L).



Figure 15: Link test pulse tail pulse mask test

Output Timing Jitter

The timing jitter at the output of the MAU is determined by measuring the timing of the zero crossings of the signal relative to the start of a data packet. The start-of-packet is found by triggering the oscilloscope on the first unit interval (bit time) after the beginning of the packet. The jitter of the edge 8 bits from this point is measured and reported in parameter P1 below the grid.

A random bit stream from the device is used for this test, and two jitter measurements are made: one on the transition at 8 bits from the trigger and the other at the transition at 8.5 bits from the trigger. The transitions represent TD1 and TD0 values respectively and are indicated in the user interface as 8 BT and 8.5 BT, respectively. In either case (TD1 or TD0) the jitter shall be less than 22 ns as indicated in parameter P1. The output jitter is measured with and without the twisted pair model and terminated into a 100 ohm resistive load.

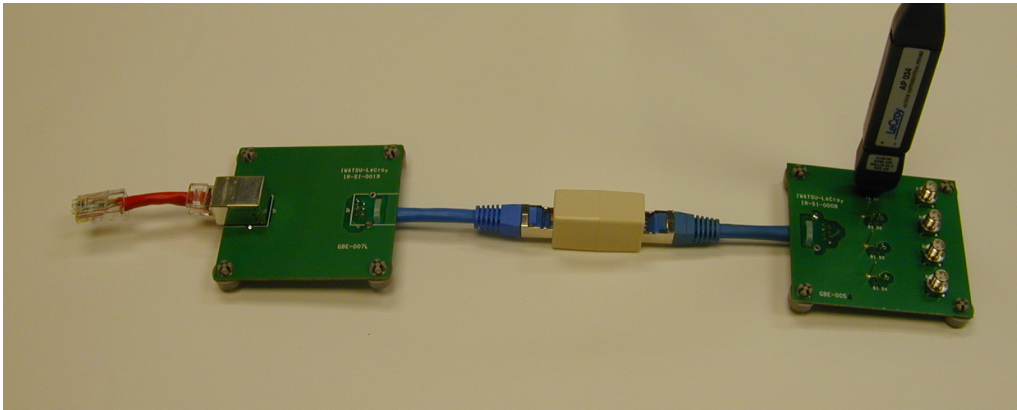


Figure 16: Fixture setup for jitter test. The twisted pair model (GBE-007) is shown on the left. The load shown is GBE-005A; however, only load GBE-001 is used. The device under test is connected to the RJ45 jack at the left side of the picture. The test is performed with and without the TP model.

1. Connect the twisted pair model fixture to the output of the DUT and connect the output of the TP model to fixture GBE001.
2. Attach the differential probe to the pins marked **TX D1** on the GBE-001 test fixture.
3. Set the DUT to transmit a random bit stream.

Note: the DUT can be set to transmit random data by connecting the DUT to a link partner and transmitting a large file to the partner. Use the GBE002L fixture for this purpose. In this case, the TP model is not used.

4. Touch the **10Base-T** button in the “Select Standard” field.
5. Enter the channel to which the differential probe is connected in the “Source for + Data” field.
6. Select **Output Timing Jitter 8 BT** in the “Select Test” field.
7. Select **external** or **integrated** MAU as appropriate in the “MAU Type” field.
8. Touch the **Set Up and Start Test** button to begin testing. The screen will display a rising edge. This is the transition of the 8th bit if that bit is a TD1. If there is not a TD1 at this bit position, no edge is displayed and no measurement is taken.
9. The measurement displayed in P1 is the peak-to-peak value of the variation in the location of the transition.
10. Select **Output Timing Jitter 8.5 BT** in the “Select Test Field.”
11. Select **external** or **integrated** MAU as appropriate in the “MAU Type” field.
12. Touch the **Set Up and Start Test** button to begin testing.
13. The measurement displayed in P1 is the peak-to-peak value of the variation in the location of the transition.

14. Remove the twisted pair model from the DUT and connect the GBE-001 fixture directly to the DUT.
15. Select **external** or **integrated** MAU as appropriate in the “MAU Type” field.
16. Touch the **Set Up and Start Test** button to begin testing.
17. The measurement displayed in P1 is the peak-to-peak value of the variation in the location of the transition.

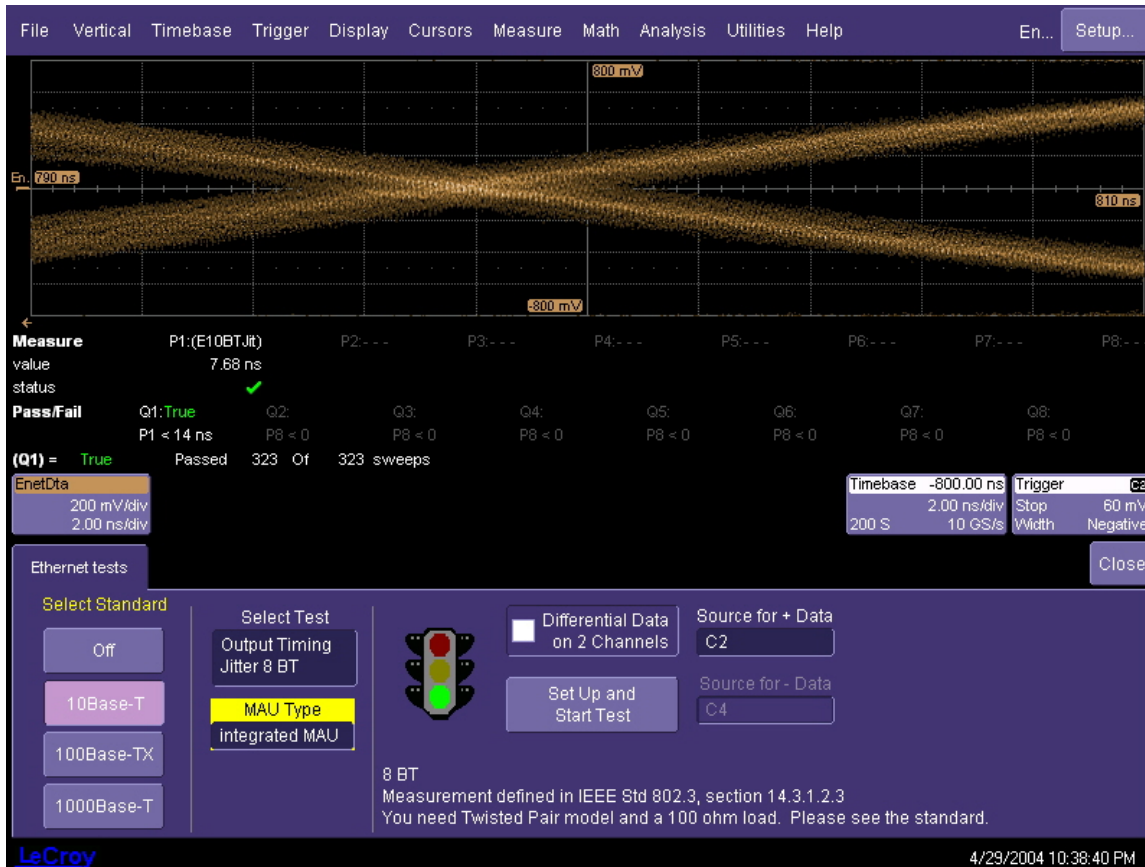


Figure 17: Output Timing Jitter 8 Bit Time Periods from Trigger

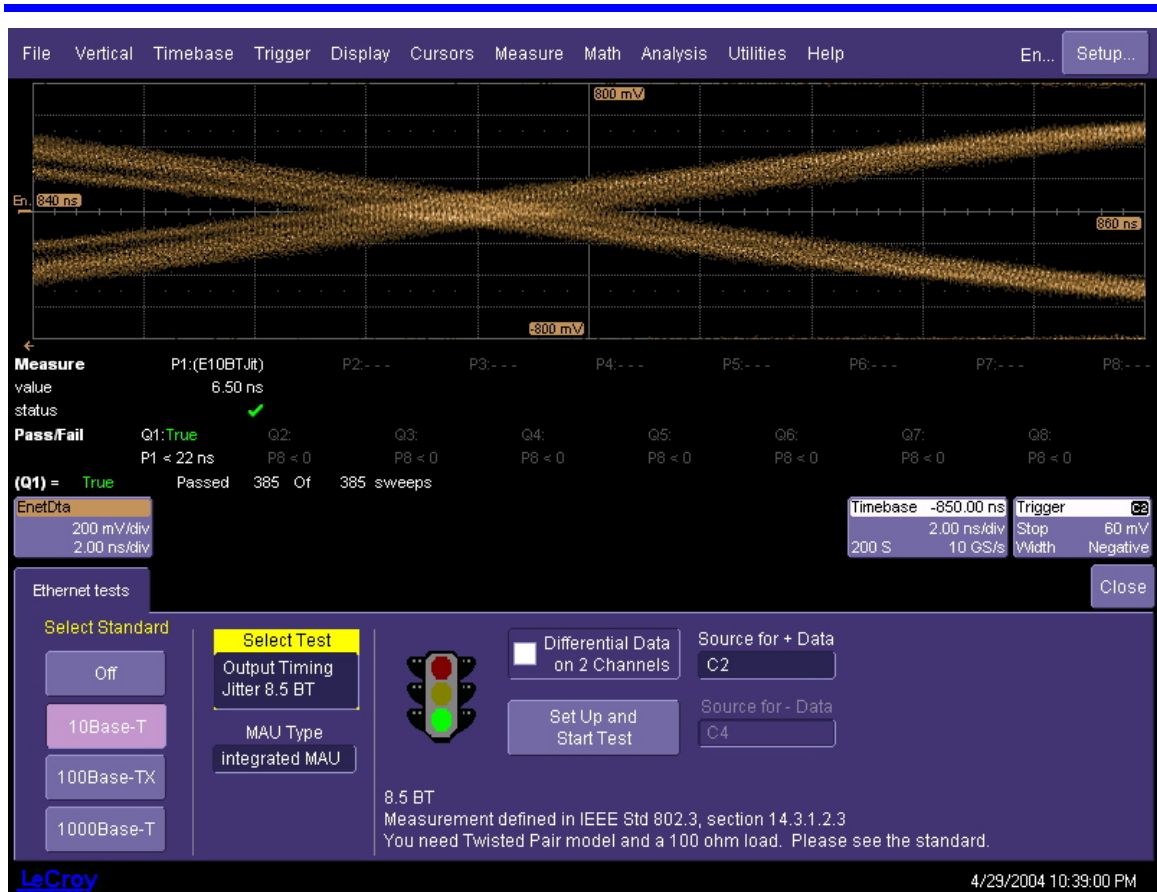


Figure 18: Output Timing Jitter 8.5 Bit Times from Trigger

100Base-TX Tests

The 100Base-TX signal is an MLT-3 signal, that is, symbols are encoded into one of three voltage levels on the twisted pair (+1, 0, and -1 V). The electrical requirements for this signal are defined in the ANSI X3.263-1995 standard for FDDI interfaces. Five tests are described in this standard and are performed in the LeCroy ENET package. These are

- Mask Test
- Jitter
- Duty Cycle Distortion
- Amplitude Measurements
- Rise and Fall Time

Connecting the oscilloscope to the device under test

The most accurate method of attaching the oscilloscope to the device under test is by directly connecting the fixture to the oscilloscope channels using a pair of SMA cables. The fixture marked GBE-004B is used for this purpose. The connections to the oscilloscope should be made with good quality SMA cables of equal length. If the tests are being performed on a WavePro or WaveRunner oscilloscope which have only BNC connections, an SMA to BNC adaptor will be required for each channel.

1. Connect the device under test to the RJ45 jack on the fixture marked GBE-004B using the short section of CAT5 cable supplied in the TF-ENET fixture kit.
2. Connect an SMA cable to the port marked TX D1+ on the fixture and a second SMA cable of equal length to the port marked TX D1- on the fixture.
3. Connect the cable from the TX D1+ port to channel 1 of the oscilloscope and the other cable to channel 2
4. Using the Vertical menu on the oscilloscope, set the coupling to “DC50 Ω ” and the offset to 0V.
5. Set the device under test to transmit a 100Base-TX signal.

Note: The test pattern needed will depend on the test to be performed and how to make a device generate this pattern is implementation specific. Please consult your Ethernet PHY device manufacturer for information on setting the device to transmit the specific test patterns. The ENET software will also perform measurements on any arbitrary data pattern from the device under test. Specific patterns are called out in this procedure where they are required by the standard.

6. Adjust the level of the signal on channel 1 until it completely fills the grid on the oscilloscope screen (about 7.5 divisions). You will need to select “Variable Gain” in the **Volts/Div** control in the vertical menu. This will give the maximum dynamic range to the measurement.
7. Set the vertical scale on channel 2 to the same value as that in channel 1 after the signal in channel 1 has been set in step 6.

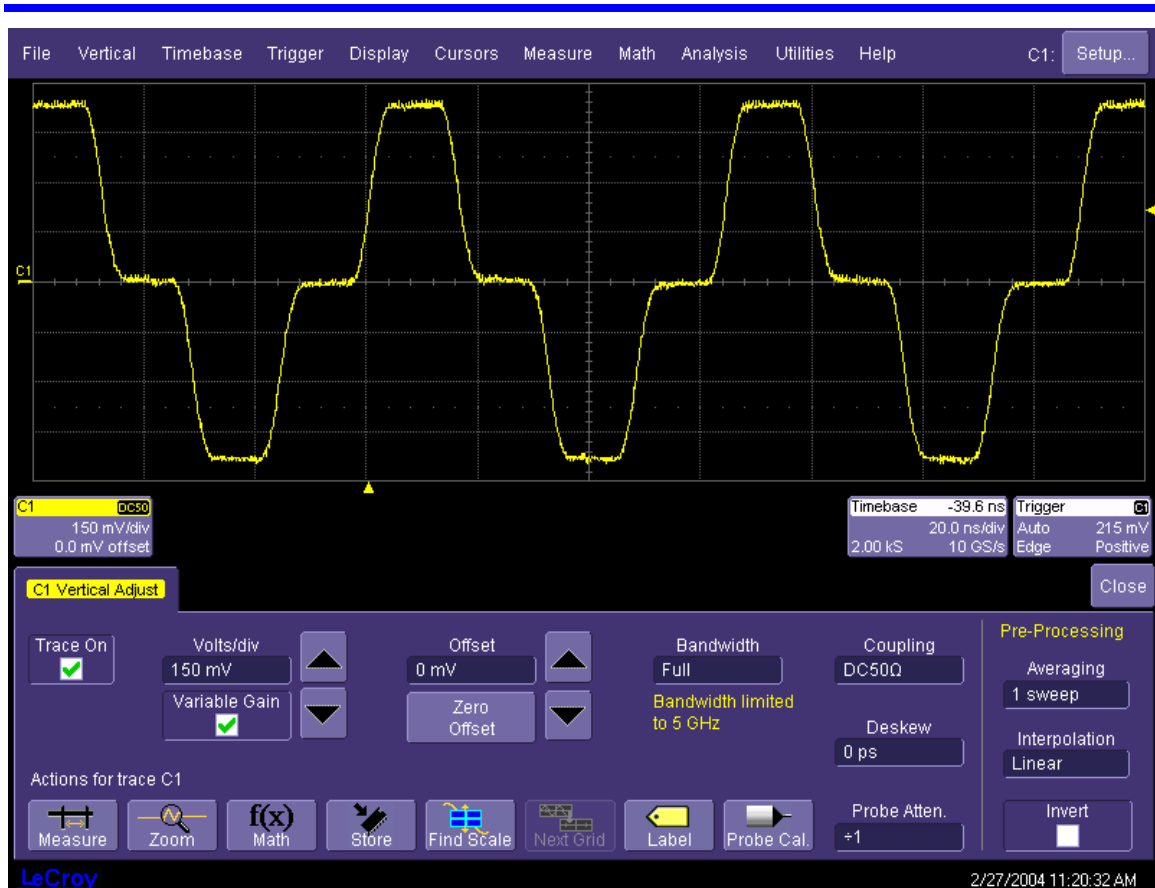


Figure 19: Adjustment of vertical scale and coupling. The signal should be adjusted using the Volts/div control to fill the grid. Note the green checkmark in the Variable Gain control which allows settings to be adjusted in 1mV steps.

Mask Test

Mask testing of 100Base-TX signals is a useful and quick method to determine the signal quality. While it is not strictly required by the 802.3 and ANSI specifications, it is commonly used because a compliant signal will not have any mask failures. More detailed analysis is required for compliance, however, because non-compliant signals may not exhibit mask failures.

1. Set the device under test to transmit the IDLE 100Base-TX data pattern. This pattern is transmitted by the interface whenever there is no communication to a link partner.
2. Touch the **100Base-TX** button under “Select Standard.”
3. Select “Differential Data on 2 Channels”
4. Enter **C1** in the “Source for + Data” control and **C2** in the “Source for – Data” control

5. Select **Mask Test** in the “Select Test” field.
6. Touch the **Set Up and Start Test** button to begin mask testing.
7. The position of the signal relative to the mask can be adjusted by the **Alignment Adj.** control if the mask does not line up properly in the horizontal direction.
8. Q1 will indicate the pass/fail condition, and a running count of the number of passed sweeps out of the total is displayed.



Figure 20: 100Base-TX Mask Test. Note that this display is achieved when the analog persistence display mode is selected

Jitter

Jitter in 100Base-TX signals is defined as the time interval error between an ideal clock at the 125 MHz symbol rate and the measured timing of the rising and falling edges of the positive and negative pulses. The reference clock is recovered from the data signal under test using a numerical PLL computed from the threshold crossings of the signal under test. The jitter test is

performed on a scrambled IDLE stream. The IDLE stream is generated by a 100Base-TX interface when it is terminated with no link partner.

1. Apply power to the device under test. An MLT3 signal trace should be displayed on the oscilloscope screen at this point.
2. Touch the **100Base-TX** button under “Select Standard.”
3. Select **Jitter** in the “Select Test” field.
4. Select “Differential Data on 2 Channels”
5. Enter **C1** in the “Source for + Data” control and **C2** in the “Source for – Data” control
6. Touch the **Set Up and Start Test** button to begin testing.
7. P1 indicates the total jitter (peak-to-peak), and the number of passing sweeps (acquisitions) out of the total is displayed.
8. The nominal bit rate is shown in the **Base Frequency** field. Click the **Find Frequency** field if the bit rate is significantly different from 125 MHz or if the jitter number is excessively large.
9. The **Average Result** checkbox, when checked, averages the measured value of p-p jitter over the number of acquisitions selected in the **Avg. Weight** field. Note that the results continue to be tested against the specified limit on each acquisition. The average is a moving window: for each acquisition up to the specified weight, the average includes one additional measurement. After the weight count is reached, the oldest value is dropped from the average and the latest measurement is added in.



Figure 21: 100Base-TX Jitter Test

Duty cycle distortion

The duty cycle distortion measurement determines the timing error on four consecutive transitions of the transmitter signal, consisting of consecutive positive and negative pulses. This MLT-3 code is generated by a 10101010... sequence. Duty cycle distortion is measured as the maximum deviation from the nominal 16 ns spacing between all of the transitions at their 50% amplitudes.

1. Apply power to the device under test. An MLT-3 signal trace should be displayed on the oscilloscope screen at this point.
2. Set the device under test to transmit a 1010... pattern.
3. Touch the **100Base-TX** button under “Select Standard.”
4. Select **Duty Cycle Distortion** in the “Select Test” field.
5. Select “Differential Data on 2 Channels”
6. Enter **C1** in the “Source for + Data” control and **C2** in the “Source for – Data” control

7. Touch the **Set Up and Start Test** button to begin testing.
8. P1 indicates the duty cycle distortion and the number of passing sweeps (acquisitions) out of the total.
9. The **Average Result** checkbox, when checked, averages measurements over the number of sweeps (acquisitions) specified in the “Avg. Weight” field.



Figure 22: 100Base-TX duty cycle distortion

Amplitude, Symmetry, and Overshoot

The peak differential voltage of the MLT-3 signal should be +/-1 V, and the overshoot of transitions must be limited to 5%. Additionally, the symmetry between the positive and negative pulses must be within 2% of each other. The overshoot value is measured by capturing the peak voltage at a transition from 0 V to 1 V (or 0 V to -1 V) and comparing this level to the mean voltage of the signal when no transitions are occurring. The waveform for this test must consist of a transition followed by 14 bit times during which the signal has no transitions.

The signal amplitude symmetry (SAS) is determined from the positive and negative peak voltage values using the following equation:

$$0.98 \leq \frac{|+V_{out}|}{| -V_{out}|} \leq 1.02$$

1. Apply power to the device under test. An MLT3 signal trace should be displayed on the oscilloscope screen at this point.
2. Set the device under test to transmit the appropriate waveform, containing transitions between 0 V and alternately +1 V and -1 V, with each state followed by 14 bit times during which no transition takes place.
3. Select **100Base-TX** in the “Select Standard” field.
4. Select **Amplitude Measurements** in the “Select Test” field.
5. Select “Differential Data on 2 Channels”
6. Enter **C1** in the “Source for + Data” control and **C2** in the “Source for – Data” control
7. Touch the **Set Up and Start Test** button to begin testing.
8. Parameter P1 indicates the differential output voltage (DOV), P2 indicates the signal amplitude symmetry (SAS), P3 indicates the overshoot for positive-going pulses, and P4 indicates the overshoot for negative-going pulses.
9. The **Average Result** checkbox, when checked, averages measurements over the number of sweeps (acquisitions) specified in the **Avg. Weight** field.

Note: Maximizing the signal on the oscilloscope screen will give the best results for this measurement. Failure to adjust the signal to its highest level may result in false failures being reported for this test.

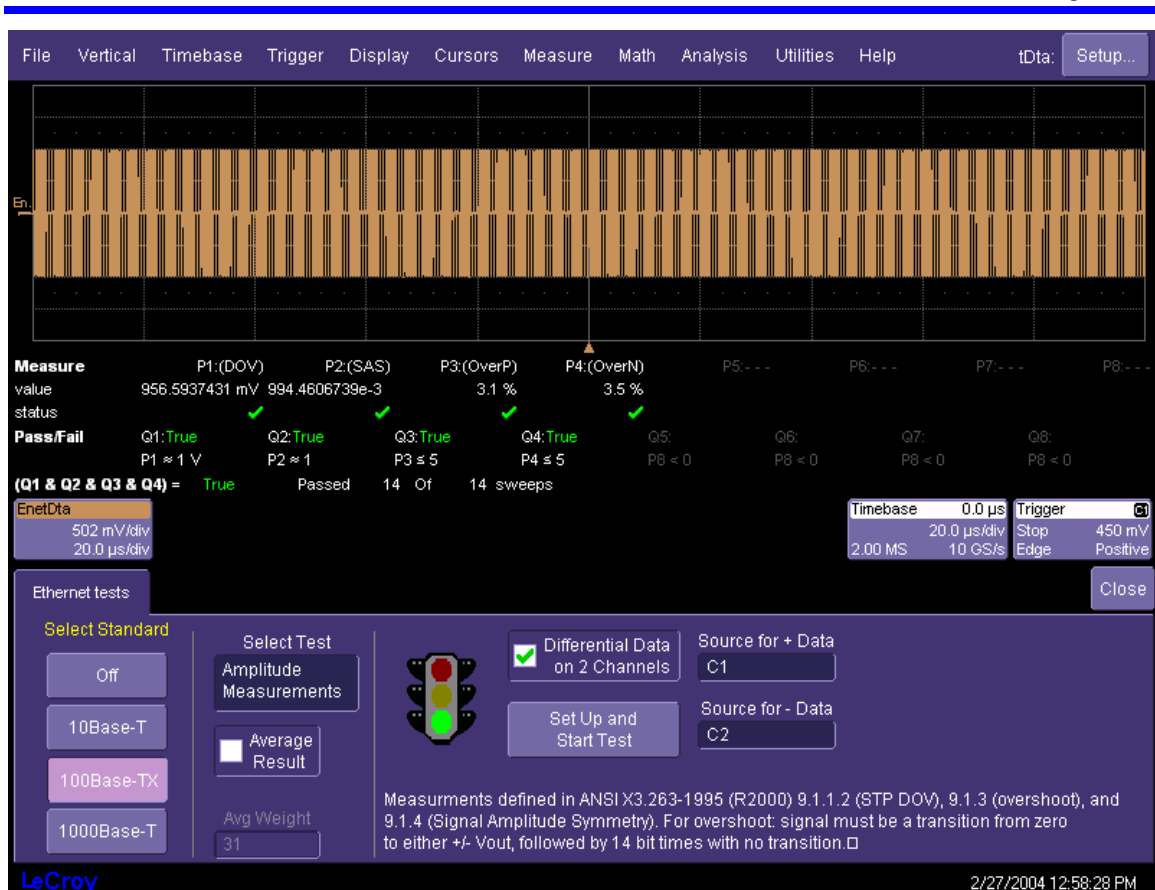


Figure 23: 100Base-TX differential output voltage and overshoot.

Rise and Fall Time

The rise time of the MLT-3 signal is defined as the transition time from the baseline (0 V) to either the positive or negative going peak, while the fall time is the time for the transition from either the positive or negative pulse to the baseline. The times are measured from the 10 to 90% levels. They are also measured for all transitions in the waveform, and must be between 3 and 5 ns. In addition, all measured values for a given transmitter must be within 0.5 ns of each other.

1. Apply power to the device under test. An MLT3 signal trace should be displayed on the oscilloscope screen at this point.
2. Select **100Base-TX** in the "Select Standard" field.
3. Select **Rise/Fall Measurements** in the "Select Test" field.
4. Select "Differential Data on 2 Channels"

5. Enter **C1** in the “Source for + Data” control and **C2** in the “Source for – Data” control
6. Touch the **Set Up and Start Test** button to begin testing.
7. Parameters P1 through P7 display the results of this test. P1 and P2 give the rise and fall times for positive-going pulses and P3 and P4 are the rise and fall times for negative-going pulses. Parameters P5 and P6 give the minimum and maximum rise/fall measurements and P7 gives the range between these values.
8. The **Average Result** checkbox is grayed out in this mode, since averaging is not applicable to this measurement.

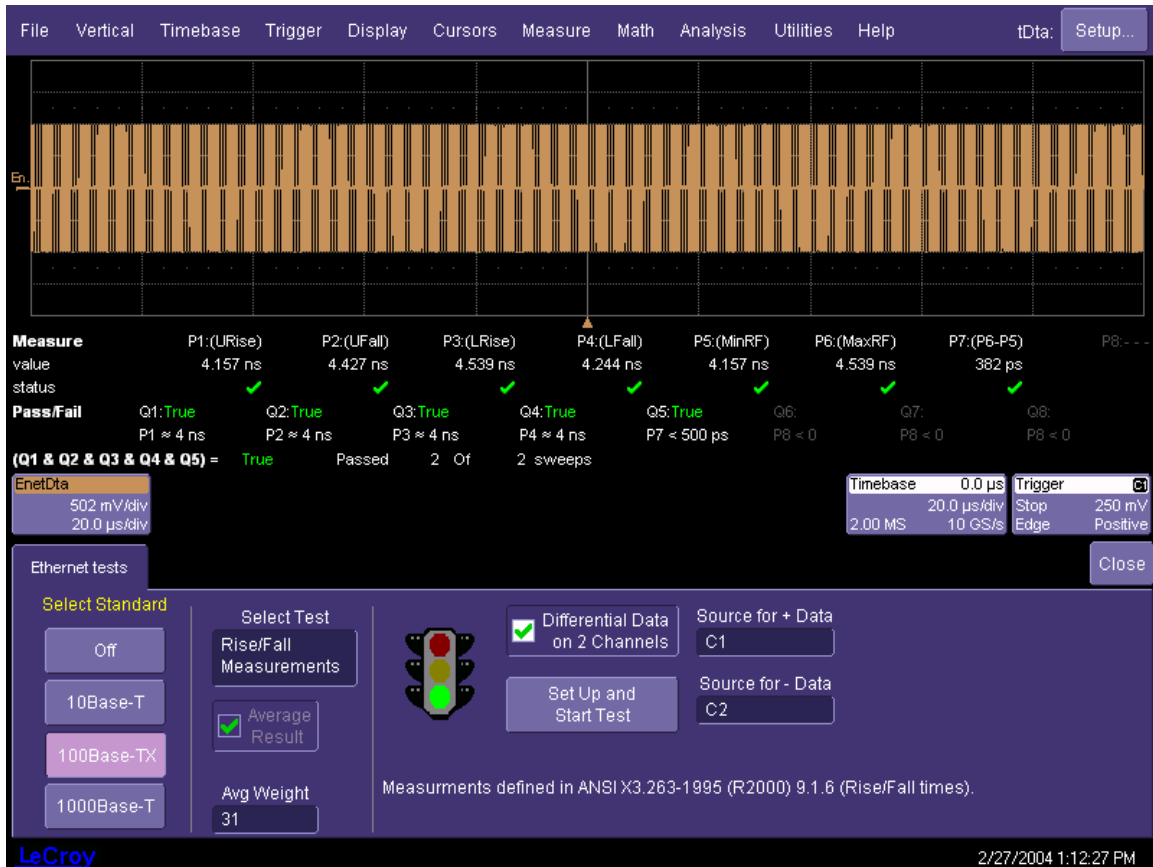


Figure 24: 100Base-TX Rise and Fall Time

1000Base-T Measurements

Transmitter measurements for gigabit Ethernet over copper (1000Base-T) are defined in the IEE802.3ab standard in clause 40.6. Four test modes are required in the physical layer device and 4 test fixtures are used to measure the four test modes, as described in Table 1. A disturbing sine wave is required for modes 1 and 4. The frequency and amplitude of this sine wave for each mode is also listed in Table 1. The test fixtures described in Table 1 and in the standard are not physical fixtures. They are test setups that include mechanical fixtures, a disturbing signal, and a (digital) filter. The fixtures are shown in schematic form below.

Table 1: Gigabit Ethernet tests, modes and fixtures

Test	Test mode	Fixture	Disturbing Sine Wave
Peak differential output voltage	1	1	31.25 MHz/2.8 V _{p-p}
Maximum output droop	1	2	31.25 MHz/2.8 V _{p-p}
Differential output templates	1	1	31.25 MHz/2.8 V _{p-p}
Transmitter distortion	4	3	20.833 MHz/5.4 V _{p-p}
Jitter in master mode	2	4	N/A
Jitter in slave mode	3	4	N/A

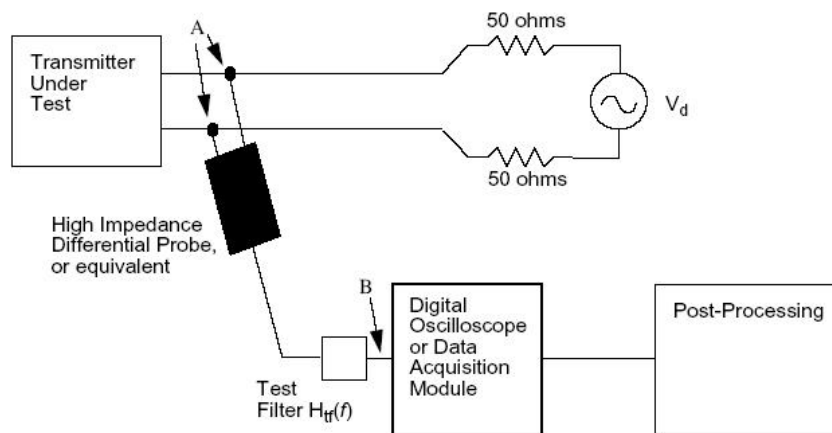


Figure 25: Test Fixture 1 Used for Mask Test and Peak Differential Voltage

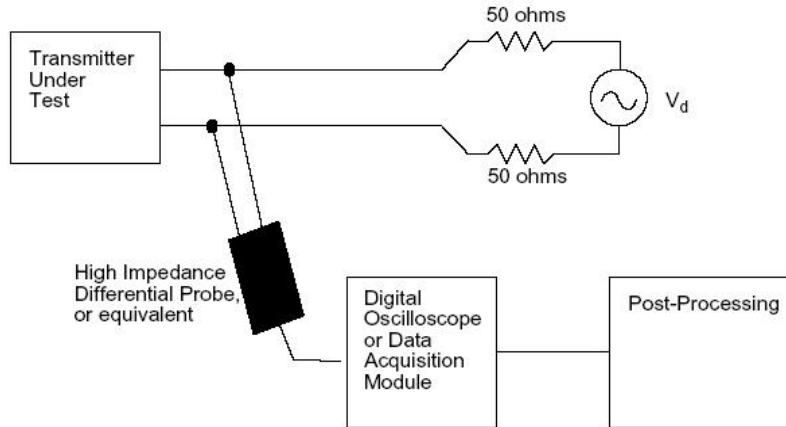


Figure 26: Test Fixture 2 Used for Droop Test

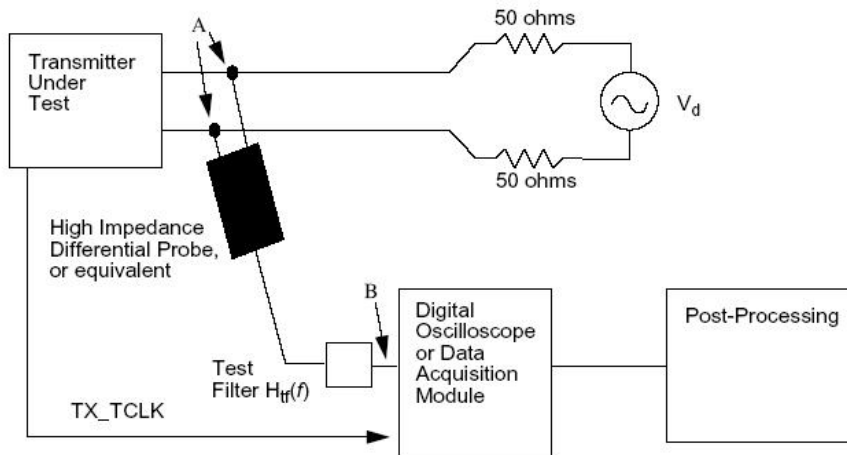


Figure 27: Test Fixture 3 Used for Transmitter Distortion

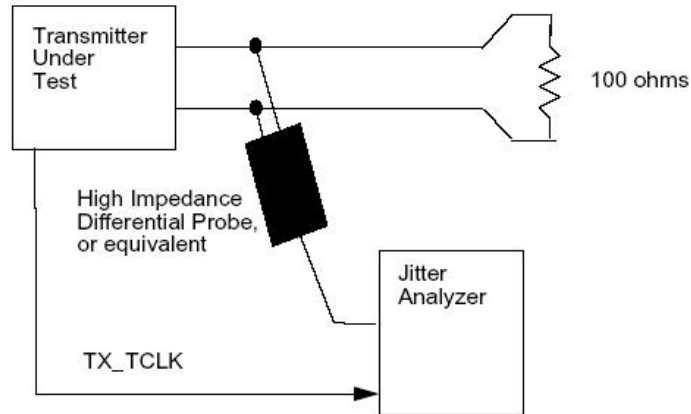


Figure 28: Test Fixture 4 Used for Jitter Tests

Peak Differential Voltage, Droop and Template Test

This test is performed on a physical interface transmitting the mode 1 waveform. Test Fixture 1 is used to perform the peak voltage and template tests while Test Fixture 2 is used for the droop test. The only difference between Test Fixtures 1 and 2 is the test filter ($H_{if}(s)$). This filter is applied using DSP in the measurement software. The disturbing sine wave is required for these tests, but in some cases it may be convenient to perform this measurement without the disturbing signal. If a disturbing signal is not used, the measurement should be made with the device terminated into a 100 ohm resistive load.

Note: The method for putting a particular PHY device into this and the other test modes required for 1000Base-T tests is unique to the manufacturer. Contact the manufacturer of your PHY device for information on how to do this.

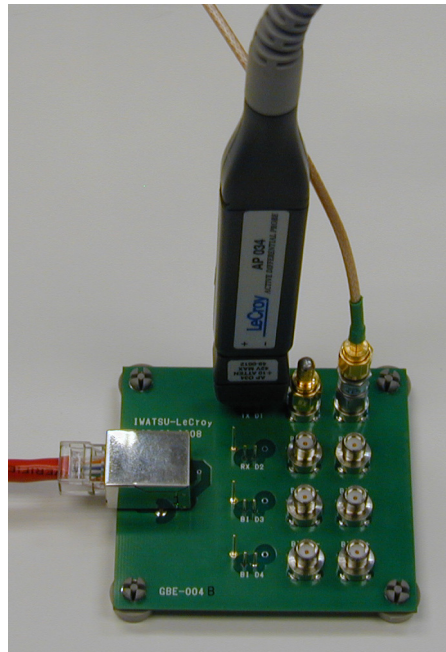


Figure 29: Connections for direct probing a 1000Base-T Mode 1 test. The power splitters are supplied with the TF-ENET fixture set.

1. Connect the output of the device under test to the fixture marked GBE-004B using the short section of CAT5 cable.
2. Attach terminators (supplied with the TF-ENET fixture) to port 1 of each splitter and connect the differential outputs of the disturbing signal generator to port 2 of the splitters, as shown in Figure 29.
3. Connect port 3 of one splitter to channel 1 of the oscilloscope and port 3 of the other splitter to channel 2 of the oscilloscope. Set the vertical scale on channels 1 and 2 to 50 mV/Div.
4. Create a math waveform on the oscilloscope that is the difference (Ch1- Ch2) between the two channels using the **Math -> F1 Setup...** menu, and display this waveform.
5. Create a parameter in P1 using the **Measure -> Measure Setup** menu that displays the peak- to-peak value of F1.
6. Adjust the disturbing signal voltage level until the peak-to-peak voltage of the waveform reads 1.4 V (parameter P1).
7. Connect the fixture to the power splitters, oscilloscope and device under test, as shown in Figure 41.

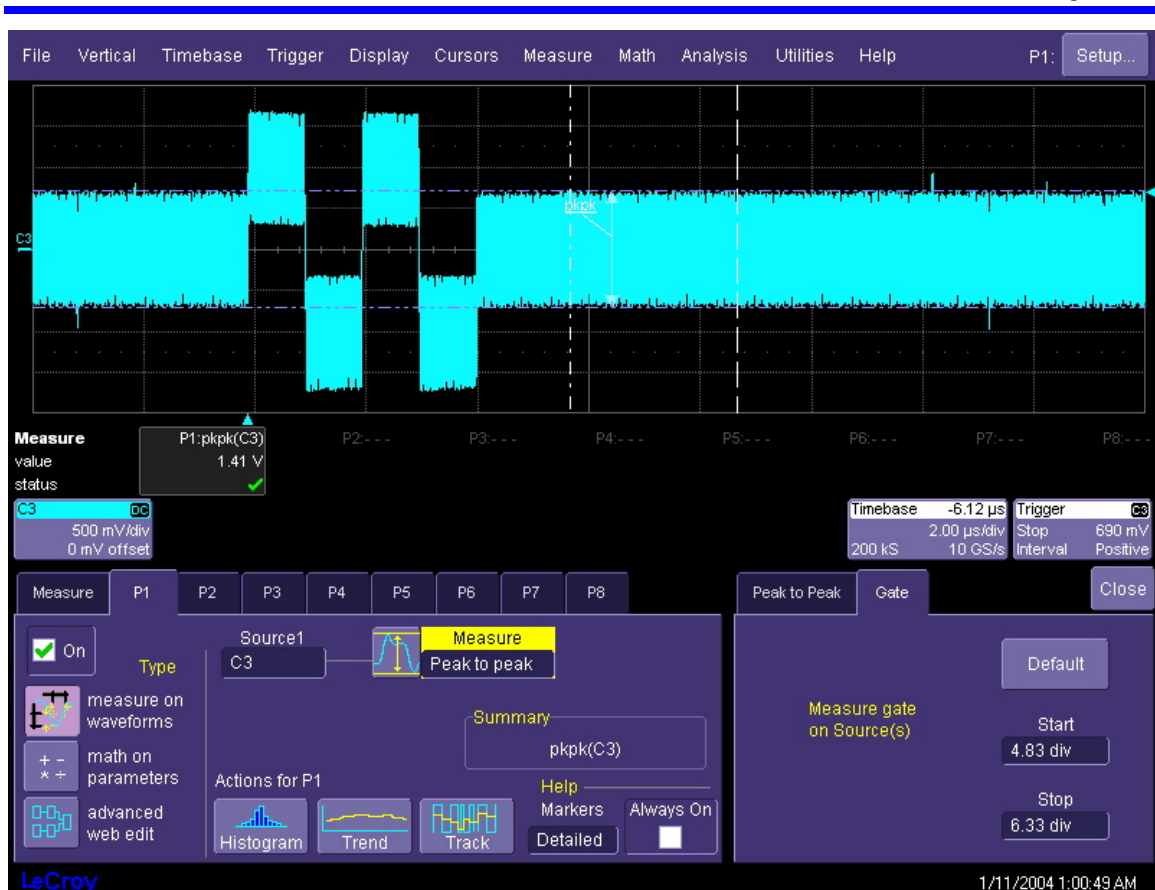


Figure 30: Setup for measuring the peak-to-peak voltage of the disturbing signal. The disturbing signal is adjusted so that the peak-to-peak voltage of the difference between channels 1 and 2 (ch1 - ch2) is 1.4 V

Note: The voltage level of 1.4 V is required because 50% of the 2.8 V from the source in the fixture is dropped across the two 50 ohm resistors shown in the diagram for Test Fixtures 1 and 2.

8. Select **1000Base-T** under “Select Standard.”
9. Select **Mode 1 Transmit Wform** in the “Select Test” field.
10. Enter the channel to which the differential probe is connected in the “Source for + Data” field.
11. Uncheck the **Set Trigger on Data Src** checkbox if you are manually triggering the oscilloscope for this test. A manual trigger must set the signal so that the wide pulse starting at point E is at the center of the screen. The trigger level will be automatically set if this control is checked.
12. Touch the **Set Up and Start Test** button to begin testing.

13. The **Average Result** checkbox is checked by default. Entering a number in the **Avg Weight** field will cause the selected number of waveforms to be averaged for each pulse (A, B, C, D, E and F).

Note: the templates used in this test have a very tight tolerance so even a small amount of noise in the measurement setup can cause mask failures. It is recommended that averaging be used to reduce the measurement noise. The waveform will look distorted and may fail the mask while the averaging is building up.

14. Parameters P1 through P4 indicate the peak differential voltages at points A, B, C, and D. P5 indicates the average absolute value of the peak voltages at A and B. P6 and P7 are the droop values.
15. The pass/fail qualifiers in Q1 through Q8 test the measurements against the standard requirements. The criteria are listed below each qualifier. More detail on each of the criteria can be viewed by clicking on the qualifier.
16. The [Mask Tests] tab shows the test results for the 6 masks defined by the standard. The [Mask Tests] table lists the test result (OK/FAIL) for each mask. Clicking on any one of the tests in the list will display the corresponding pulse with its compliance mask. Points where the curve touches the mask are highlighted by a red circle.
17. Check the [Show all Masks] control to view an octal grid displaying all of the mask tests on one screen. The two grids on the top left of the display are reserved for the oscilloscope trace and the trace filtered by the measurement filter (labeled EnetDta).

Note: the octal grid appears very small on the screen. Click the [Close] button at the top right of the menu to close it and expand the view. The menu can be re-displayed by clicking on any one of the waveform descriptor boxes at the bottom left of the display or by selecting "Ethernet tests" in the [Analysis] menu.

18. Repeat steps 2 through 16 for the other three pairs on the device. Move the terminations and disturbing signal to the corresponding SMA jacks on the fixture for each pair.

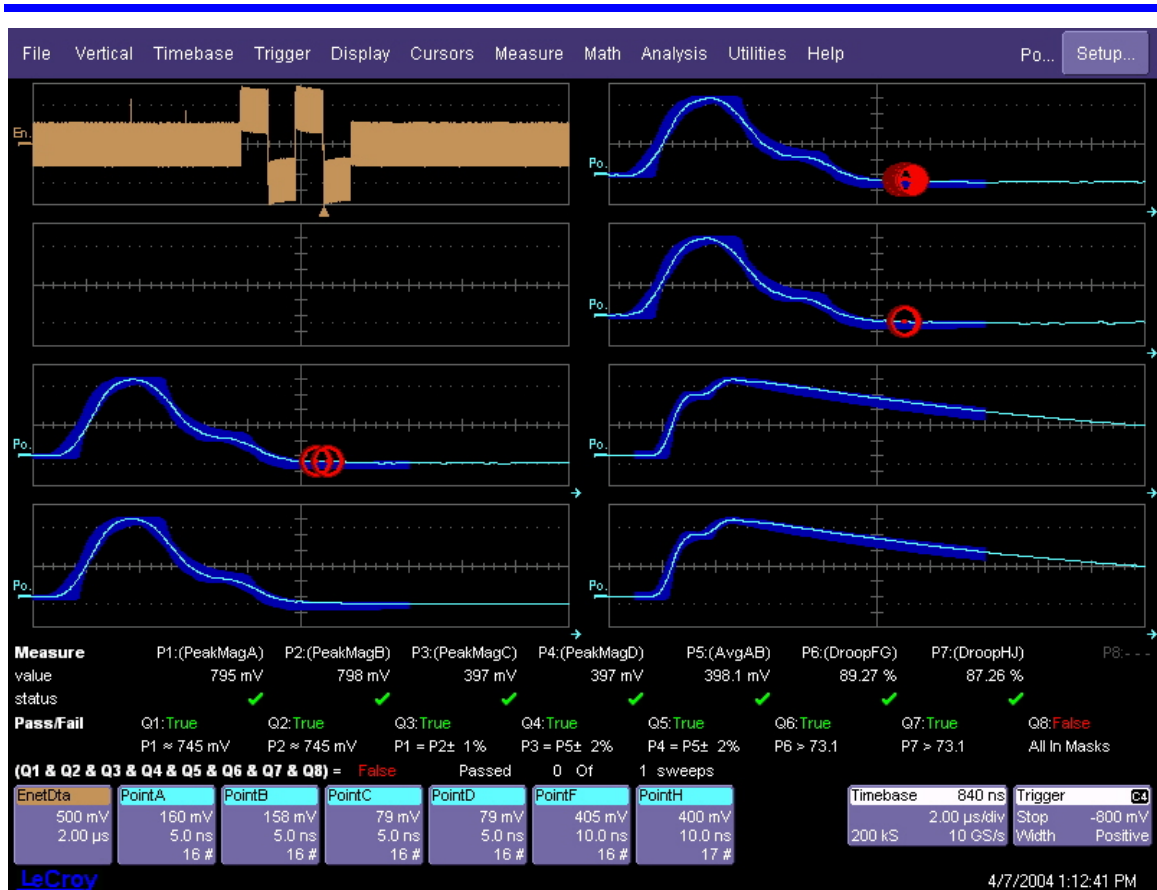


Figure 31: 1000Base-T mode 1 test showing all masks. The red circles indicate areas where the waveform touches the mask.



Figure 32: 1000Base-T mode 1 test showing one mask. The mask test results are listed in the menu

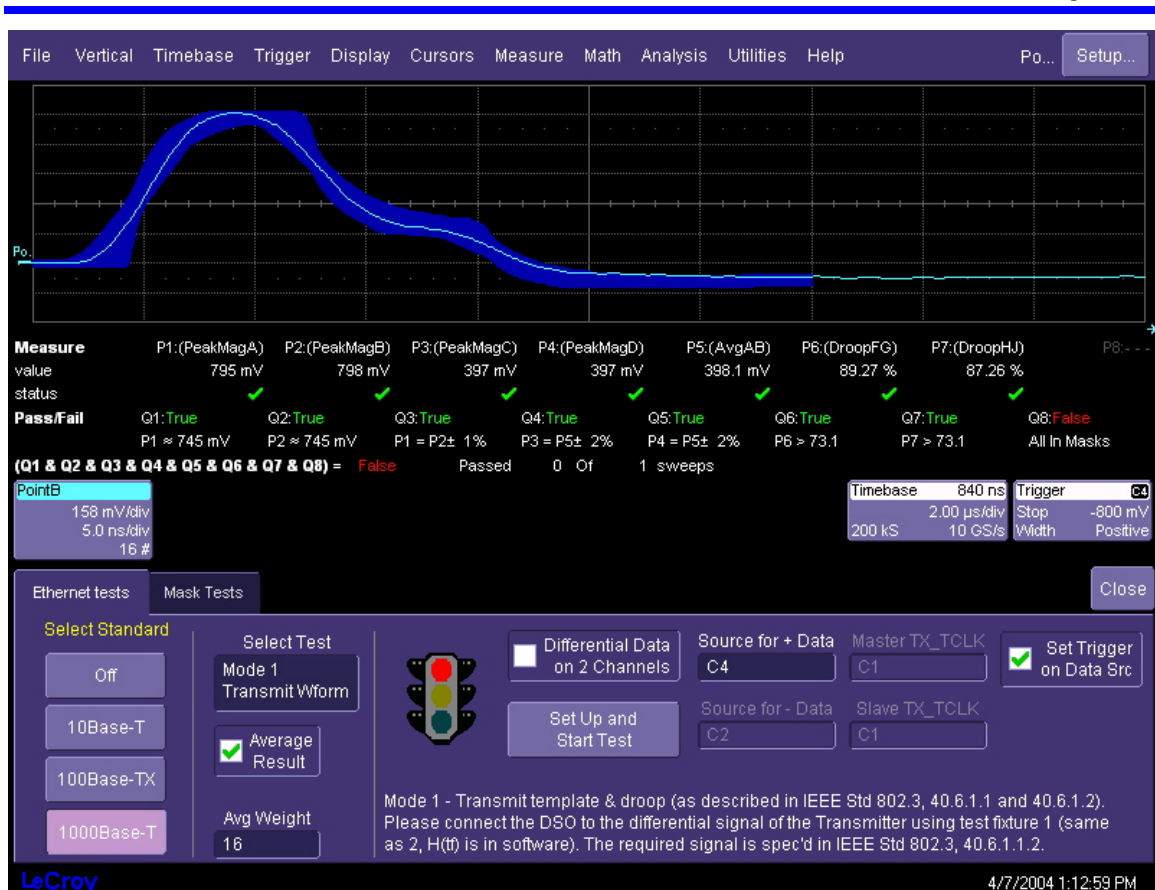


Figure 33: 1000Base-T mode 1 test main menu. The red circles indicate mask violations

Transmitter Distortion

The distortion test measures the error in the signal under test relative to an ideal waveform generated by a mathematical model of the PAM-5 coded signal. Test fixture 3 which contains the test filter and disturbing signal is used for this test. The disturbing signal is set to a frequency of 20.833MHz (125MHz/6) at a level of 5.4V (2.7V at the input to the DUT). The test requires that the absolute maximum peak error be less than 10mV.

The signal plus disturbing sine wave has a total peak to peak value of greater than 2.7V. The measurement requirement of 10mV requires that resolution exceed the normal 8 bit digitizing range of current oscilloscopes. In order to accommodate this requirement, the measurement software uses a high degree of averaging to increase the digitizing range for this measurement. The averaging requires that the signal phase as well as the phase of the disturbing sine wave be closely tracked.

Note: the averaging process requires that the phase of the disturbing sine wave be fixed relative to the waveform from the device under test. This is achieved by using a disturbing signal that is phase-locked to the 125MHz transmit clock. The averaging will give lower distortion values if this synchronization is not done.

1. Connect the output of the device under test to the fixture marked GBE-004B using the short section of CAT5 cable.
2. Attach a 50 ohm termination to the SMA jack marked TX D1- and a 6dB attenuator to the SMA jack marked TX D1+.
3. Connect the disturbing signal generator to the other side of the 6dB attenuator.
4. Attach the differential probe to the pins marked TX D1.
5. With the device under test transmitting the mode 1 waveform, turn on the disturbing signal generator and view the signal from the differential probe on the oscilloscope screen. Adjust the signal level on the signal generator until the signal observed on the oscilloscope reaches a peak to peak voltage of 2.7V.



Figure 34: Setting the disturbing signal level for mode 4 test

6. Set the device under test to transmit the mode 4 waveform.

7. adjust the Volts/div control in the Vertical menu to maximize the signal plus disturber on the oscilloscope screen.
8. Select “1000Base-T” in the **Select Standard** control.
9. Select “Mode 4 distortion” in the **Select Test** control.
10. Enter the channel to which the differential probe is connected in the **Source for + Data** control.
11. Click the **Setup and Start Test** control to begin the test.
12. The initial distortion values may be above 30mV but will quickly drop as the averaging process proceeds. The measurement will reach a minimum value and then vary around this level. Record the lowest value as the measurement result.

Note: Averaging is affected by the relative phase between the Ethernet symbols and the disturbing sine wave. It is recommended that the disturbing signal be generated in such a way as to be synchronous to the Ethernet symbol clock.

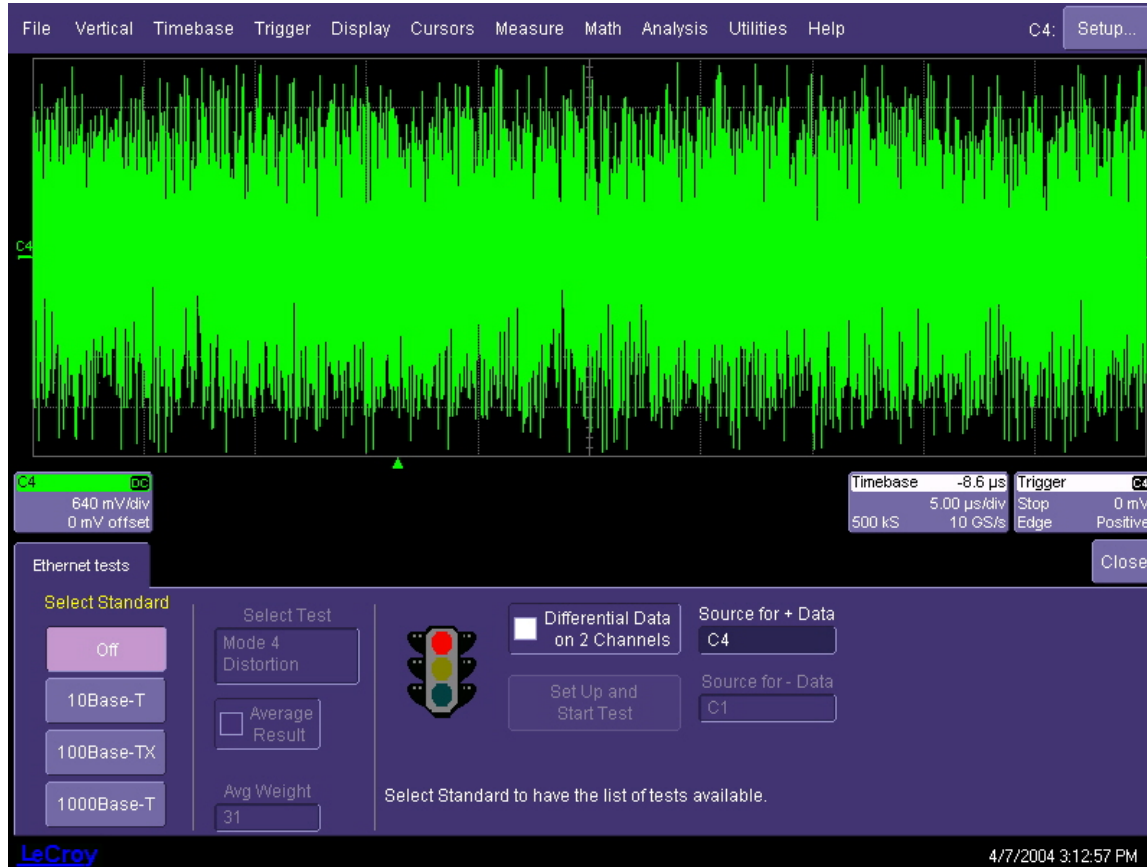


Figure 35: Level adjustment of mode 4 test signal. The waveform should be maximized on screen without exceeding the top and bottom levels

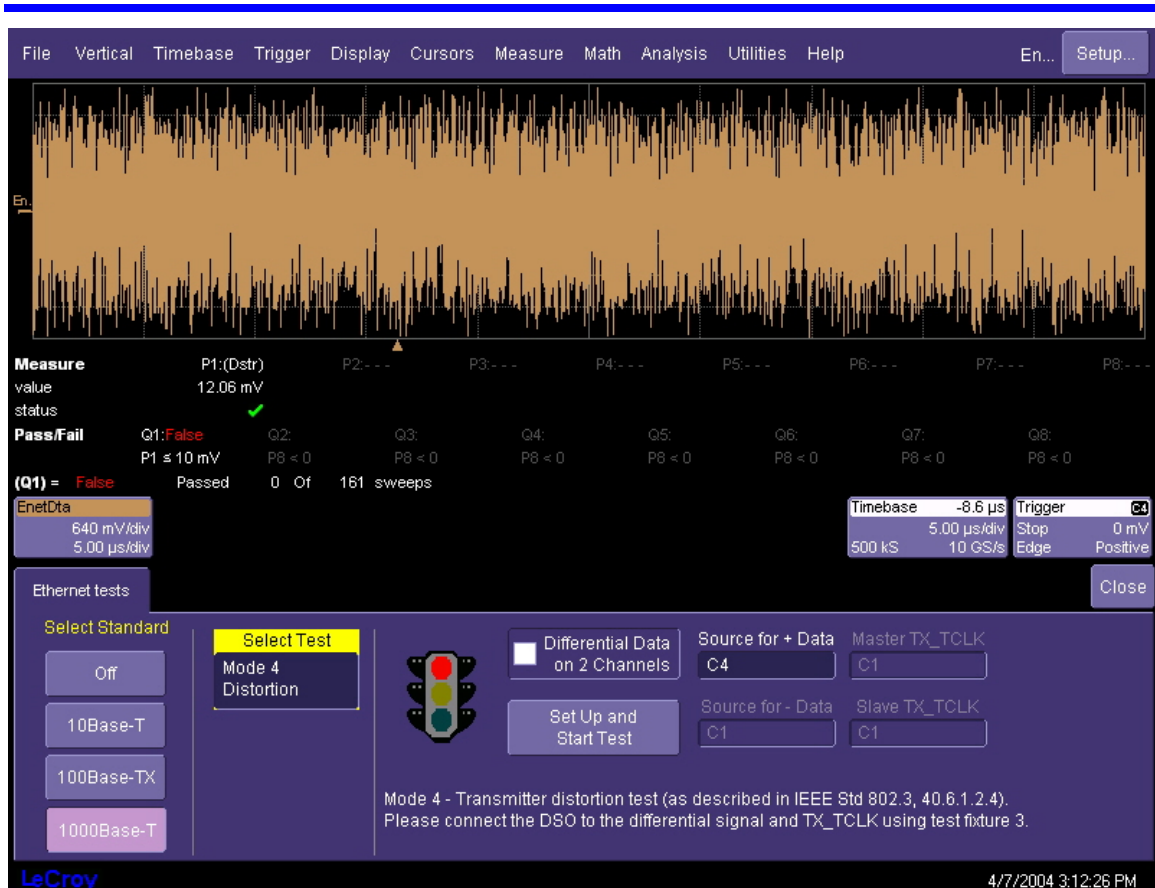


Figure 36: Mode 4 distortion measurement. Note that it is not always possible to reach the specified 10mV level without a synchronous disturbing signal

Jitter in Master Mode

Jitter in the master mode is measured with the transmitter under test terminated into a 100 ohm resistive load. The transmitter under test is set to transmit an alternating +.5, -.5V pattern. The peak to peak jitter of the output signal (on the signal output lines) relative to the corresponding transition of the transmit clock (TX_TCLK) is measured. The peak to peak jitter of the transmit clock (TX_TCLK) is also measured relative to an un-jittered reference which is derived from the average frequency of the clock. The peak to peak value of this jitter is also measured after being filtered by a 5KHz high pass filter defined in the standard.

Note: this measurement requires access to the master TX_TCLK signal. This clock can be probed on one of the pins of the PHY chip using an active probe. Contact your PHY chip vendor for information on the location of this signal.

1. Connect the output of the device under test to the fixture marked GBE004B using the short section of CAT5 cable.

2. Attach 50 ohm terminations to the SMA jacks marked TX D1- and TX D1+.
3. Attach the differential probe to the pins marked TX D1 on the fixture.
4. Attach the active voltage probe to the TX_TCLK signal.
5. Apply power to the device under test and set it to mode 2. A clock signal should appear on the channel containing the differential probe.
6. Select “1000Base-T” in the **Select Standard** control.
7. Select “Mode 2 jitter in master mode” in the **Select Test** control.
8. Enter the channel to which the differential probe is connected in the **source for + data** control.
9. Click the **setup and start test** control to begin the test.
10. Parameter P1 is the p-p jitter on the TX_TCLK relative to an un-jittered reference. The reference for this measurement is the average frequency of the clock. This frequency appears in the **Base Frequency** control. If P1 is too large, click the **Find Frequency** control to find the base frequency.
11. Parameter P2 is the p-p jitter of the data signal relative to TX_TCLK. P3 is the filtered p-p jitter the track of P1 and P4 is the sum of P2 and P3.

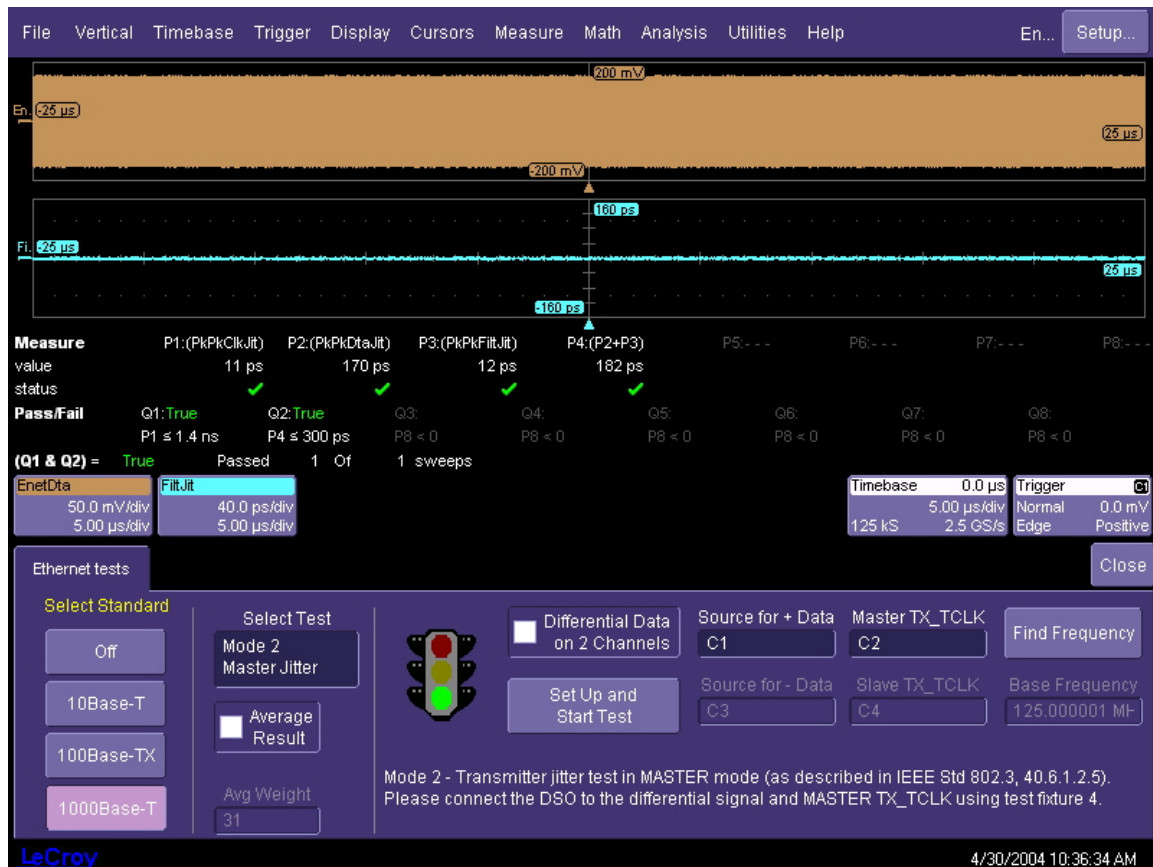


Figure 37: jitter in master mode. The upper trace shows the signal on the interface and the lower trace is the filtered jitter track of the master clock

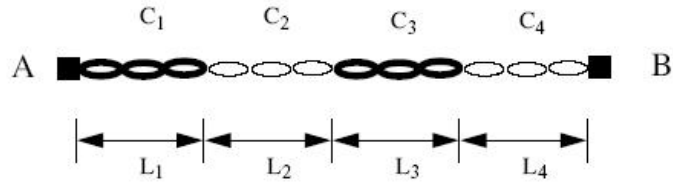
Jitter in Slave Mode

Jitter in slave mode is designed to measure the jitter in the recovered clock in the device under test relative to the reference clock in a second 1000Base-T transmitter also known as the link partner in this test. The link partner is connected to the device under test using a section of specially configured CAT5 cable as described in IEEE802.3-2000 in clause 40.6.1.1.1. The test channel description from the specification is reproduced in the figure below. The channel is built up of four sections of cable with different lengths and impedances as described in the figure. The test channel presents a worst-case connection between the master (link partner) and slave (device under test).

1. Connect the device under test to one side of the pass-through fixture (GBE-002).
2. Connect the other side of the fixture to the link partner using the test channel. If no test channel is available, a length of CAT5 cable can be used.
3. Set the device under test into test mode 3 (jitter in slave mode).

4. Attach the differential probe to the pins marked TX D1 on the fixture.
5. Using an active probe (HFP2500), probe the TX_TCLK on the device under test (slave)
6. Connect a second active probe (HFP2500) to the TX_TCLK on the link partner (master)
7. Attach the slave TX_TCLK signal to channel 2 of the oscilloscope and the master TX_TCLK to channel 3. The differential probe should be on channel 1
8. Select "1000Base-T" in the **Select Standard** control.
9. Select "Mode 3 jitter in slave mode" in the **Select Test** control.
10. Enter channel 1 in the **source for + data** control, channel 2 in the **Slave TX_TCLK** control and channel 3 in the **Master TX_TCLK** control.
11. Click the **setup and start test** control to begin the test.
12. The parameter P1 shows the p-p jitter of the slave TX_TCLK relative to the master TX_TCLK. P2 is the jitter in P1 filtered through a 33KHz high pass. P3 is the jitter of the differential signal relative to the slave TX_TCLK and P4 is the sum of P2 and P3.
13. P1 must be less than 1.4ns and the parameter P4 must be no more than 400ps greater than the value in P2 (the filtered clock jitter).

Note: The TX_TCLK signal is normally probed on one of the pins of the Ethernet PHY chip. Contact the PHY chip vendor to determine the appropriate pin to probe. In many cases, this clock is not externally available.



Identical for each of the four pairs.

Figure 40–18—Test channel topology for each cable pair

Table 40–6—Test channel cable segment specifications

Cable segment	Length (meters)	Characteristic impedance (at frequencies > 1 MHz)	Attenuation (per 100 meters at 31.25 MHz)
1	$L_1=1.20$	$120 \pm 5\Omega$	7.8 to 8.8 dB
2	$L_2=x$	$100 \pm 5\Omega$	10.8 to 11.8 dB
3	$L_3=1.48$	$120 \pm 5\Omega$	7.8 to 8.8 dB
4	$L_4=y$	$100 \pm 5\Omega$	10.8 to 11.8 dB

NOTE— x is chosen so that the total delay of segments C1, C2, and C3, averaged across all pairs, is equal to 570 ns at 31.25 MHz; however, if this would cause the total attenuation of segments C1, C2, and C3, averaged across all pairs, to exceed the worst case insertion loss specified in 40.7.2.1 then x is chosen so that the total attenuation of segments C1, C2, and C3, averaged across all pairs, does not violate 40.7.2.1 at any frequencies. The value of y is chosen so that the total attenuation of segments C1, C2, C3, and C4, averaged across all pairs, does not violate 40.7.2.1 at any frequency (y may be 0).

Figure 38: Jitter test channel definition. This cable is used to connect the device under test to the link partner



Figure 39: Jitter in slave mode. The trace shows the filtered track of the timing jitter between the master and slave transmit clock signals (TX_TCLK).

APPENDIX A: DIRECT PROBING

Even the highest quality differential probes will be non-linear and have noise levels that may be unacceptable for measuring 1000Base-T Ethernet signals. The noise and distortion in the probe will add to the signal being measured and may result in mask or distortion failures. One way to eliminate probing effects is to connect the signal under test directly to the oscilloscope inputs. By using the 50 ohm impedance of the oscilloscope channels between each signal wire and ground, a 100 ohm differential impedance across the wire pair is achieved. This configuration gives the ideal compliance load and eliminates the probe and its distortions. The LeCroy Ethernet fixtures (TF-ENET) are configured to support this type of probing.

Attaching the Signal to the Oscilloscope

On the test fixture marked GBE-004B, connect the SMA jack marked “TX D1+” to channel 1 of the oscilloscope using an SMA cable. Similarly, connect the jack marked “TX D1-“ to channel 2 of the oscilloscope using an SMA cable. If the oscilloscope has selectable input impedance, select the 50 ohm setting for channels 1 and 2. This is not necessary for the WaveMaster and SDA. Check the [Differential Data on Two Channels] control in the ENET control panel and enter channel 1 in the [Source for + Data] control and channel 2 in the [Source for – Data] control. Connect the RJ45 connector on the fixture to the output of the device under test.

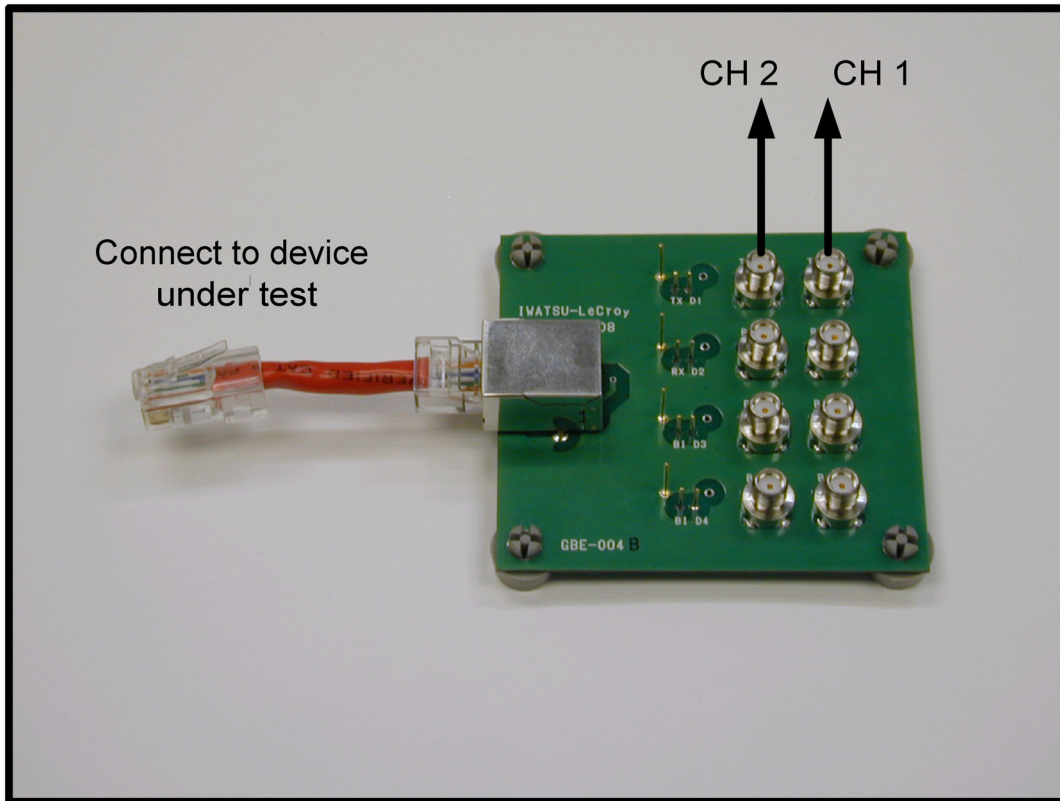


Figure 40: Connection points for direct connection to oscilloscope channels

Connecting the Disturbing Signal

In order to support mode 1 and mode 4 tests, a disturbing signal is required. The disturbing signal is applied through a pair of hybrid power splitters. The power splitters allow the disturbing signal to be applied to the device under test at its full voltage level while attenuating it at the port connected to the oscilloscope. The power splitter also maintains the required 50 ohm impedance between each wire and ground. A hybrid power splitter contains 3 ports; one input and two outputs. Each output carries one half of the signal power present at the input. The signal flow between the two outputs is highly attenuated due to the directional nature of the ports.

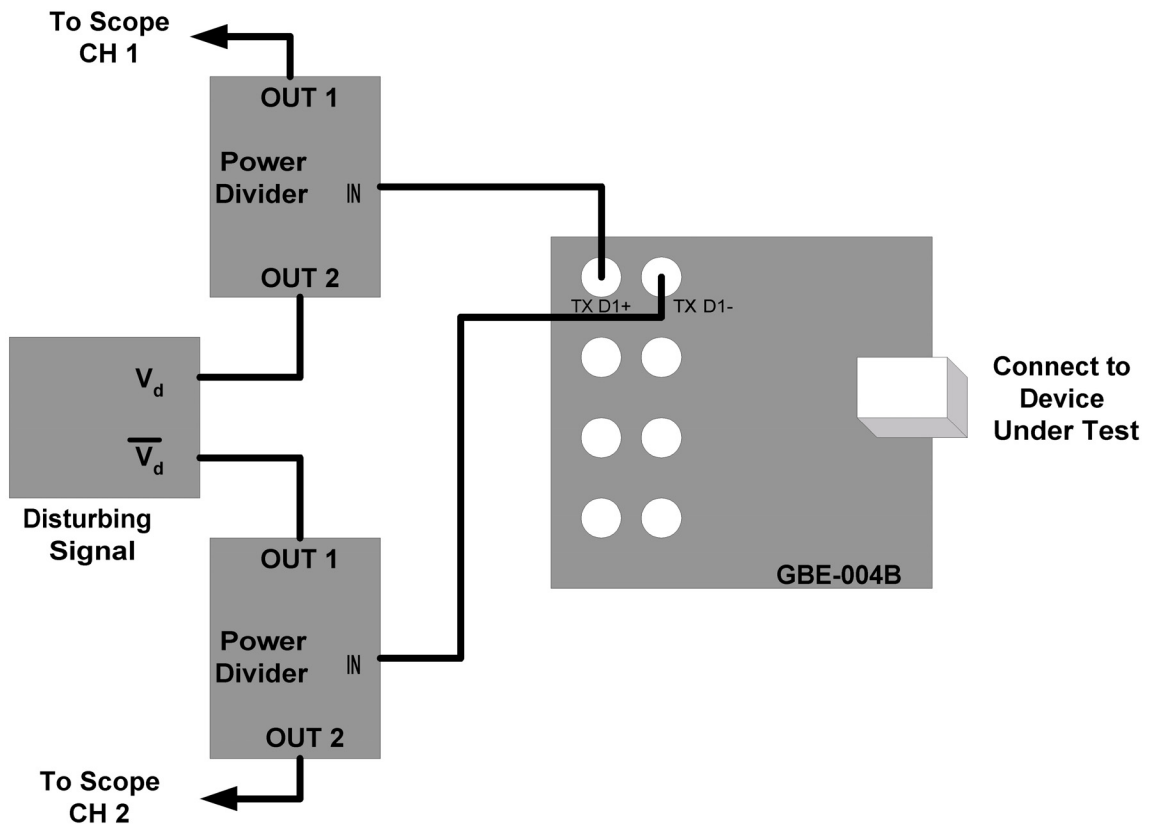


Figure 41: Connections for Disturbing Signal for Modes 1 and 4

Note: Do not use resistive dividers to connect the disturbing signal. This type of divider provides no isolation between the disturbing signal and the oscilloscope.

The amplitude of the disturbing signal can be set by monitoring the mode 1 signal as described in this manual. Use a differential probe connected to the TX D1 pins in the fixture to monitor the mode 1 signal and, using a gated measurement, measure the peak to peak voltage and adjust it to the appropriate level for the test as listed in Table 1. Connect the differential probe to an unused channel (3 or 4 in this case) and measure the disturbing signal level with all of the other connections in place. The measured disturbing signal levels should be one-half of the values listed in Table 1.

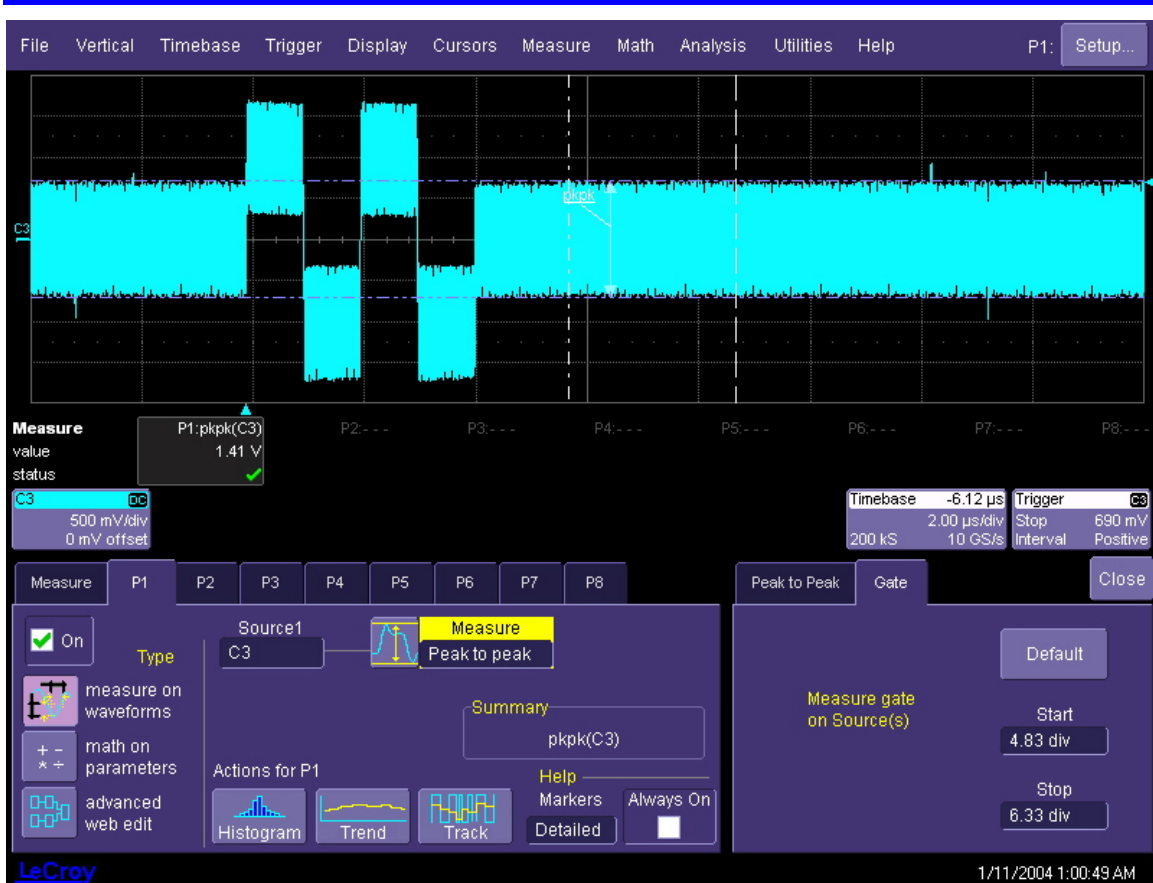


Figure 42: Measuring the Disturbing Signal Level

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